

# MPC8548E PowerQUICC™ III Integrated Processor Hardware Specifications

## 1 Overview

This section provides a high-level overview of MPC8548E features. [Figure 1](#) shows the major functional units within the MPC8548E.

Although this document is written from the perspective of the MPC8548E, most of the material applies to the other family members—MPC8547E, MPC8545E, and MPC8543E—as well. When specific differences occur, such as pinout differences and processor frequency ranges, they will be identified as such.

For specific PVR and SVR numbers, refer to the *MPC8548E Integrated Host Processor Reference Manual*.

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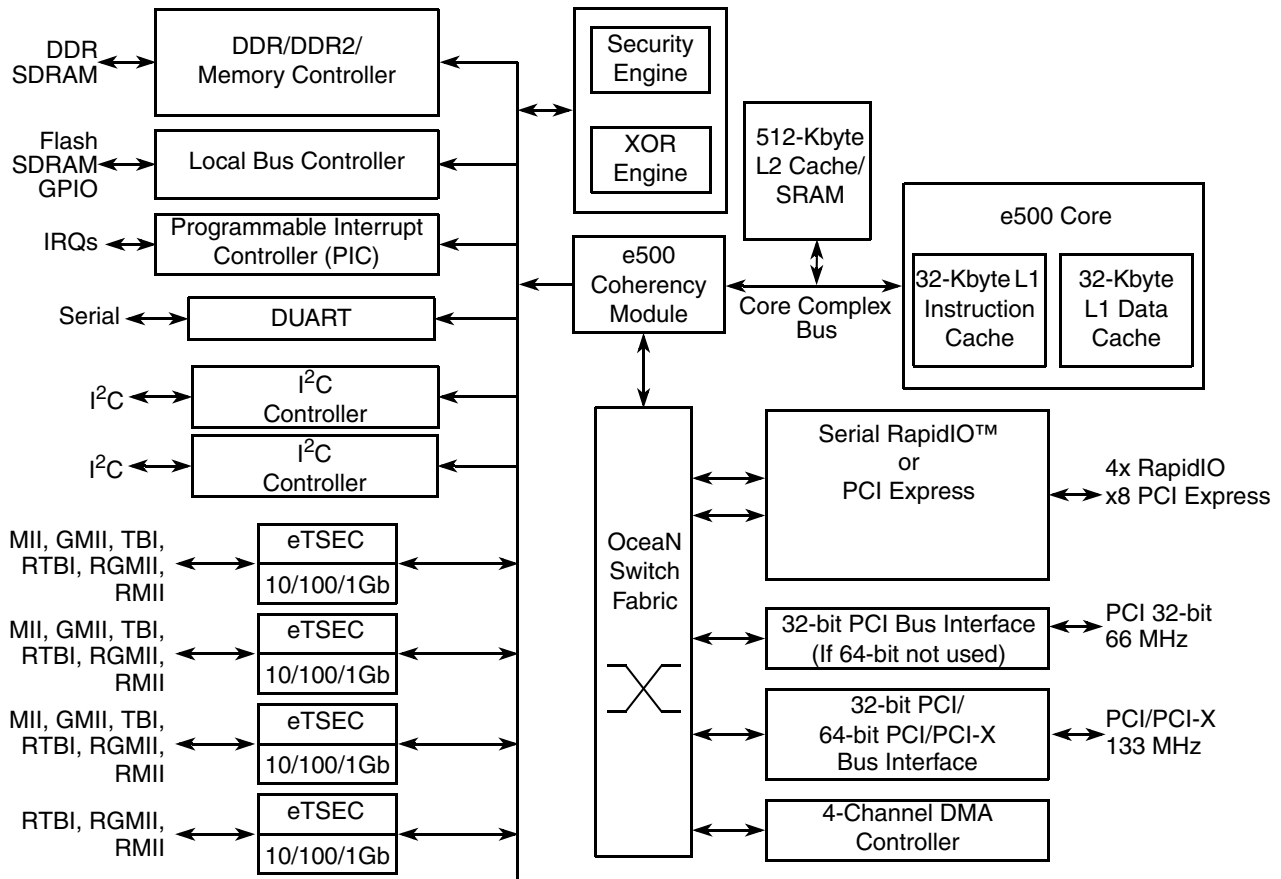


Figure 1. MPC8548E Block Diagram

## 1.1 Key Features

The following list provides an overview of the MPC8548E feature set:

- High-performance 32-bit core built on Power Architecture™ technology.
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
  - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - 36-bit real addressing
  - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
  - Enhanced hardware and software debug support

- Performance monitor facility that is similar to, but separate from, the MPC8548E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
  - Flexible configuration.
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
  - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
    - Four inbound windows plus a default window on RapidIO™
    - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
    - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface
  - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Full ECC support
  - Page mode support
    - Up to 16 simultaneous open pages for DDR

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL\_2 compatible I/O (1.8-V SSTL\_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with  $F_2^m$  and  $F(p)$  modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES

- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I<sup>2</sup>C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I<sup>2</sup>C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I<sup>2</sup>C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I<sup>2</sup>C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT,  $\overline{\text{RTS}}$ ,  $\overline{\text{CTS}}$ )
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers designed to comply with IEEE Std. 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3ac™, 802.3ab™
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE Std. 802.3 GMII, IEEE Std. 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE Std. 802.3 MII, IEEE Std. 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
    - Up to 16 exact-match MAC addresses supported
    - Broadcast address (accept/reject)

- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  - PCI 2.2 and PCI-X 1.0 compatible
  - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible

- Selectable hardware-enforced coherency
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification, Revision 1.2*
  - Both 1x and 4x LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
  - Auto detection of 1x- and 4x-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO\_READ\_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO-compliant message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox
  - Single inbound doorbell message structure
  - Facility to accept port-write messages



- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports x8, x4, x2, and x1 link widths
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high speed I/O interfaces supports one of the following configurations:
  - x8 PCI Express
  - x4 PCI Express and 4x serial RapidIO
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the eight counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1™

## 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8548E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

### 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

#### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings <sup>1</sup>

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		$V_{DD}$	-0.3 to 1.21	V	
PLL supply voltage		$AV_{DD}$	-0.3 to 1.21	V	
Core power supply for SerDes transceivers		$SV_{DD}$	-0.3 to 1.21	V	
Pad power supply for SerDes transceivers		$XV_{DD}$	-0.3 to 1.21	V	
DDR and DDR2 DRAM I/O voltage		$GV_{DD}$	-0.3 to 2.75 -0.3 to 1.98	V	2
Three-speed Ethernet I/O, MII management voltage		$LV_{DD}$ (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	3
		$TV_{DD}$ (for eTSEC3 and eTSEC4)	-0.3 to 3.63 -0.3 to 2.75		3
PCI/PCI-X, DUART, system control and power management, I <sup>2</sup> C, and JTAG I/O voltage		$OV_{DD}$	-0.3 to 3.63	V	
Local bus I/O voltage		$BV_{DD}$	-0.3 to 3.63 -0.3 to 2.75	V	
Input voltage	DDR/DDR2 DRAM signals	$MV_{IN}$	-0.3 to ( $GV_{DD} + 0.3$ )	V	4
	DDR/DDR2 DRAM reference	$MV_{REF}$	-0.3 to ( $GV_{DD}/2 + 0.3$ )	V	
	Three-speed Ethernet signals	$LV_{IN}$ $TV_{IN}$	-0.3 to ( $LV_{DD} + 0.3$ ) -0.3 to ( $TV_{DD} + 0.3$ )	V	4
	Local bus signals	$BV_{IN}$	-0.3 to ( $BV_{DD} + 0.3$ )		
	DUART, SYSClk, system control and power management, I <sup>2</sup> C, and JTAG signals	$OV_{IN}$	-0.3 to ( $OV_{DD} + 0.3$ )	V	4
	PCI/PCI-X	$OV_{IN}$	-0.3 to ( $OV_{DD} + 0.3$ )	V	4

**Table 1. Absolute Maximum Ratings <sup>1</sup> (continued)**

Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T <sub>STG</sub>	-55 to 150	•C	

**Notes:**

- Functional and tested operating conditions are given in [Table 2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- The -0.3 to 2.75 V range is for DDR and -0.3 to 1.98 V range is for DDR2.
- The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See [Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications”](#) for details on the recommended operating conditions per protocol.
- (M,L,O)V<sub>IN</sub> and MV<sub>REF</sub> may overshoot/undershoot to a voltage and for a maximum duration as shown in [Figure 2](#).

## 2.1.2 Recommended Operating Conditions

[Table 2](#) provides the recommended operating conditions for this device. Note that the values in [Table 2](#) are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

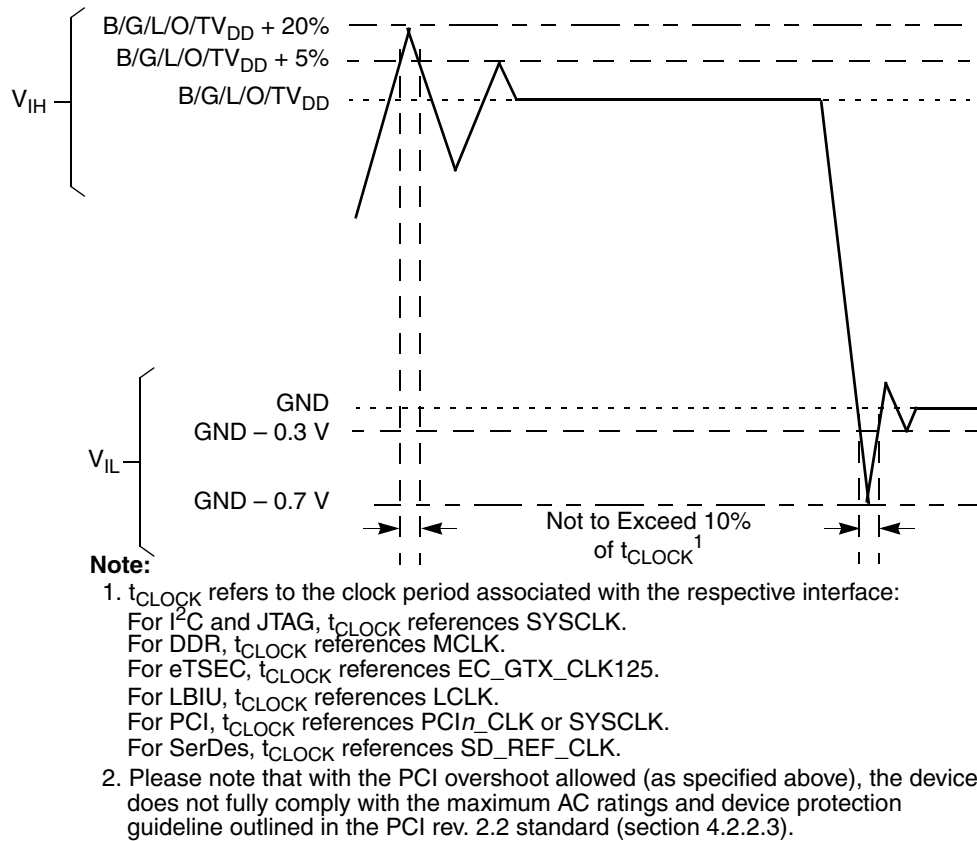
**Table 2. Recommended Operating Conditions**

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V <sub>DD</sub>	1.1 V ± 55 mV	V	
PLL supply voltage		AV <sub>DD</sub>	1.1 V ± 55 mV	V	1
Core power supply for SerDes transceivers		SV <sub>DD</sub>	1.1 V ± 55 mV	V	
Pad power supply for SerDes transceivers		XV <sub>DD</sub>	1.1 V ± 55 mV	V	
DDR and DDR2 DRAM I/O voltage		GV <sub>DD</sub>	2.5 V ± 125 mV 1.8 V ± 90 mV	V	
Three-speed Ethernet I/O voltage		LV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV		4
PCI/PCI-X, DUART, system control and power management, I <sup>2</sup> C, and JTAG I/O voltage		OV <sub>DD</sub>	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV	V	
Input voltage	DDR and DDR2 DRAM signals	MV <sub>IN</sub>	GND to GV <sub>DD</sub>	V	2
	DDR and DDR2 DRAM reference	MV <sub>REF</sub>	GND to GV <sub>DD</sub> /2	V	2
	Three-speed Ethernet signals	LV <sub>IN</sub> TV <sub>IN</sub>	GND to LV <sub>DD</sub> GND to TV <sub>DD</sub>	V	4
	Local bus signals	BV <sub>IN</sub>	GND to BV <sub>DD</sub>	V	
	PCI, Local bus, DUART, SYSCLK, system control and power management, I <sup>2</sup> C, and JTAG signals	OV <sub>IN</sub>	GND to OV <sub>DD</sub>	V	3

**Table 2. Recommended Operating Conditions (continued)**

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T <sub>J</sub>	0 to 105	°C	
<b>Notes:</b> 1. This voltage is the input to the filter discussed in <a href="#">Section 21.2.1, “PLL Power Supply Filtering”</a> and not necessarily the voltage at the AV <sub>DD</sub> pin, which may be reduced from V <sub>DD</sub> by the filter. 2. <b>Caution:</b> MV <sub>IN</sub> must not exceed GV <sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. 3. <b>Caution:</b> OV <sub>IN</sub> must not exceed OV <sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. 4. <b>Caution:</b> L/TV <sub>IN</sub> must not exceed L/TV <sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.				

Figure 2 shows the undershoot and overshoot voltages at the interfaces of this device.



**Figure 2. Overshoot/Undershoot Voltage for GV<sub>DD</sub>/OV<sub>DD</sub>/LV<sub>DD</sub>/BV<sub>DD</sub>/TV<sub>DD</sub>**

The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in [Table 2](#). The input voltage threshold scales with respect to the associated I/O supply voltage. OV<sub>DD</sub> and LV<sub>DD</sub> based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV<sub>REF</sub> signal (nominally set to GV<sub>DD</sub>/2) as is appropriate for the SSTL2 electrical signaling standard.

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

Driver Type	Programmable Output Impedance ( $\Omega$ )	Supply Voltage	Notes
Local bus interface utilities signals	25	$BV_{DD} = 3.3\text{ V}$	1
	25	$BV_{DD} = 2.5\text{ V}$	
PCI signals	45(default)	$BV_{DD} = 3.3\text{ V}$	2
	45(default)	$BV_{DD} = 2.5\text{ V}$	
DDR signal	25	$OV_{DD} = 3.3\text{ V}$	3
	45(default)		
DDR2 signal	18	$GV_{DD} = 2.5\text{ V}$	3
	36 (half strength mode)		
TSEC/10/100 signals	18	$GV_{DD} = 1.8\text{ V}$	3
	36 (half strength mode)		
TSEC/10/100 signals	45	$L/TV_{DD} = 2.5/3.3\text{ V}$	
DUART, system control, JTAG	45	$OV_{DD} = 3.3\text{ V}$	
I2C	150	$OV_{DD} = 3.3\text{ V}$	

**Notes:**

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the  $\overline{PCI\_GNT1}$  signal at reset.
3. The drive strength of the DDR interface in half-strength mode is at  $T_j = 105^\circ\text{C}$  and at  $GV_{DD}$  (min).

## 2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

1.  $V_{DD}$ ,  $AV_{DD-n}$ ,  $BV_{DD}$ ,  $LV_{DD}$ ,  $OV_{DD}$ ,  $SV_{DD}$ ,  $TV_{DD}$ ,  $XV_{DD}$
2.  $GV_{DD}$

All supplies must be at their stable values within 50 ms.

**NOTE**

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

**NOTE**

In order to guarantee MCKE low during power-up, the above sequencing for  $GV_{DD}$  is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for  $GV_{DD}$  is not required.

**NOTE**

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

### 3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in [Table 4](#).

**Table 4. MPC8548E Power Dissipation**

CCB Frequency <sup>1</sup>	Core Frequency	SLEEP <sup>2</sup>	Typical-65 <sup>3</sup>	Typical-105 <sup>4</sup>	Maximum <sup>5</sup>	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	W
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

**NOTES:**

1. CCB Frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on  $V_{DD} = 1.1$  V,  $T_j = 65$  °C.
3. Typical-65 is based on  $V_{DD} = 1.1$  V,  $T_j = 65$  °C, running Dhrystone.
4. Typical-105 is based on  $V_{DD} = 1.1$  V,  $T_j = 105$  °C, running Dhrystone.
5. Maximum is based on  $V_{DD} = 1.1$  V,  $T_j = 105$  °C, running a smoke test.

Because I/O usage varies from design to design, power dissipation *estimates* for the I/O supplies are provided in [Table 5](#).

**Table 5. MPC8548E Estimated I/O Power Dissipation**

Interface	Parameters	1.1 V ( $XV_{DD}$ )	1.8 V ( $GV_{DD}$ )	2.5 V ( $B/G/L/TV_{DD}$ )	3.3 V ( $B/L/O/TV_{DD}$ )	Comments
DDR	266 MHz data		0.31 W	0.59 W		
	333 MHz data		0.38 W	0.73 W		
	400 MHz data		0.46 W			
	533 MHz data		0.60 W			
PCI-Express	x8, 2.5 G-baud	0.71 W				
Serial RapidIO	x4, 3.125 G-baud	0.49 W				
PCI-X	64-bit, 133 MHz				0.25 W	
PCI	64-bit, 66 MHz				0.14 W	
	64-bit, 33 MHz				0.08 W	
	32-bit, 66 MHz				0.07 W	Power per PCI port
	32-bit, 33 MHz				0.04 W	

Table 5. MPC8548E Estimated I/O Power Dissipation

Interface	Parameters	1.1 V (XV <sub>DD</sub> )	1.8 V (GV <sub>DD</sub> )	2.5 V (B/G/L/TV <sub>DD</sub> )	3.3 V (B/L/O/TV <sub>DD</sub> )	Comments
Local Bus	32-bit, 133 MHz			0.14 W	0.24 W	
	32-bit, 66MHz			0.07 W	0.13 W	
	32-bit, 33 MHz			0.04 W	0.07 W	
eTSEC (10/100/1000 Ethernet)	MII				0.01 W	Power per eTSEC used
	GMII				0.07 W	
	TBI				0.07 W	
	RGMII			0.04 W		
	RTBI			0.04 W		
eTSEC (packet FIFO)	16-bit, 200 MHz			0.20 W		Power per FIFO interface used
	16-bit, 155 MHz			0.16 W		
	8-bit, 200 MHz			0.11 W		
	8-bit, 155 MHz			0.08 W		

## 4 Input Clocks

### 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8548E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$ .

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	$f_{\text{SYSCLK}}$	16	—	133	MHz	1, 6
SYSCLK cycle time	$t_{\text{SYSCLK}}$	7.5	—	60	ns	6
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

#### Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- This parameter has been adjusted slower according to the workaround for device erratum GEN-13.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{CCB}$ , and minimum clock low time is  $2 \times t_{CCB}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.

## 4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC\_GTX\_CLK125) AC timing specifications for the MPC8548E.

**Table 7. EC\_GTX\_CLK125 AC Timing Specifications**

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	$f_{G125}$	—	125	—	MHz	
EC_GTX_CLK125 cycle time	$t_{G125}$	—	8	—	ns	
EC_GTX_CLK125 rise and fall time L/TVDD=2.5V L/TVDD=3.3V	$t_{G125R}$ , $t_{G125F}$		—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	$t_{G125H}/t_{G125}$	45 47	—	55 53	%	2, 3

**Notes:**

- Rise and fall times for EC\_GTX\_CLK125 are measured from 0.5V and 2.0V for L/TV<sub>DD</sub>=2.5V, and from 0.6 and 2.7V for L/TV<sub>DD</sub>=3.3V.
- Timing is guaranteed by design and characterization.
- EC\_GTX\_CLK125 is used to generate the GTX clock TSEC<sub>n</sub>\_GTX\_CLK for the eTSEC transmitter with 2% degradation. EC\_GTX\_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC<sub>n</sub>\_GTX\_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications" for duty cycle for 10Base-T and 100Base-T reference clock.

## 4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCI<sub>n</sub>\_CLK. Table 8 provides the PCI/PCI-X reference clock AC timing specifications for the MPC8548E.

**Table 8. PCI<sub>n</sub>\_CLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with OV<sub>DD</sub> = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI <sub>n</sub> _CLK frequency	$f_{PCICLK}$	16	—	133	MHz	—
PCI <sub>n</sub> _CLK cycle time	$t_{PCICLK}$	7.5	—	60	ns	—
PCI <sub>n</sub> _CLK rise and fall time	$t_{PCIKH}$ , $t_{PCIKL}$	0.6	1.0	2.1	ns	1, 2



**Table 8. PCI<sub>n</sub>\_CLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3\text{ V} \pm 165\text{ mV}$ .

PCI <sub>n</sub> _CLK duty cycle	$t_{PCIHKHL}/t_{PCICLK}$	40	—	60	%	2
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**Notes:**

1. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
2. Timing is guaranteed by design and characterization.

## 4.5 Platform to FIFO restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency} / 4.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz

For FIFO encoded mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency} / 3.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

## 4.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{500\text{ MHz} \times (\text{PCI-Express link width})}{8}$$

See *MPC8548ERM, Rev. 2*, Section 18.1.3.2, “Link Width,” for PCI Express interface width details.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

See *MPC8548ERM, Rev. 2*, Section 17.4, “1x/4x LP-Serial Signal Descriptions,” for serial RapidIO interface width and frequency details.

## 4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform see the specific section of this document.

## 5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8548E. [Table 9](#) provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

**Table 9. RESET Initialization Timing Specifications**

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	$\mu\text{s}$	
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYCLKs	1
PLL input setup time with stable SYCLK before $\overline{\text{HRESET}}$ negation	100	—	$\mu\text{s}$	
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYCLKs	1

**Notes:**

1. SYCLK is the primary clock input for the MPC8548E.

[Table 10](#) provides the PLL lock times.

**Table 10. PLL Lock Times**

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	$\mu\text{s}$	
Local bus PLL lock time	—	50	$\mu\text{s}$	
PCI/PCI-X bus PLL lock time	—	50	$\mu\text{s}$	

## 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8548E. Note that  $GV_{DD}(\text{typ}) = 2.5 \text{ V}$  for DDR SDRAM, and  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$  for DDR2 SDRAM.

### 6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR2 SDRAM controller of the MPC8548E when  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$ .

**Table 11. DDR2 SDRAM DC Electrical Characteristics for  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	$GV_{DD}$	1.71	1.89	V	1
I/O reference voltage	$MV_{REF}$	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	$V_{TT}$	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	$V_{IH}$	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	$MV_{REF} - 0.125$	V	
Output leakage current	$I_{OZ}$	-50	50	$\mu\text{A}$	4
Output high current ( $V_{OUT} = 1.420 \text{ V}$ )	$I_{OH}$	-13.4	—	mA	
Output low current ( $V_{OUT} = 0.280 \text{ V}$ )	$I_{OL}$	13.4	—	mA	

**Notes:**

- $GV_{DD}$  is expected to be within 50 mV of the DRAM  $V_{DD}$  at all times.
- $MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed  $\pm 2\%$  of the DC value.
- $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to  $MV_{REF}$ . This rail should track variations in the DC level of  $MV_{REF}$ .
- Output leakage is measured with all outputs disabled,  $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$ .

Table 12 provides the DDR2 I/O capacitance when  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$ .

**Table 12. DDR2 SDRAM Capacitance for  $GV_{DD}(\text{typ})=1.8 \text{ V}$**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	$C_{IO}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	$C_{DIO}$	—	0.5	pF	1

**Note:**

- This parameter is sampled.  $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$ ,  $f = 1 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

Table 13 provides the recommended operating conditions for the DDR SDRAM controller when  $GV_{DD}(\text{typ}) = 2.5 \text{ V}$ .

Table 13. DDR SDRAM DC Electrical Characteristics for  $GV_{DD}$  (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	$GV_{DD}$	2.375	2.625	V	1
I/O reference voltage	$MV_{REF}$	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	$V_{TT}$	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	$V_{IH}$	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	$MV_{REF} - 0.15$	V	
Output leakage current	$I_{OZ}$	-50	50	$\mu A$	4
Output high current ( $V_{OUT} = 1.95$ V)	$I_{OH}$	-16.2	—	mA	
Output low current ( $V_{OUT} = 0.35$ V)	$I_{OL}$	16.2	—	mA	

**Notes:**

- $GV_{DD}$  is expected to be within 50 mV of the DRAM  $V_{DD}$  at all times.
- $MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed  $\pm 2\%$  of the DC value.
- $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to  $MV_{REF}$ . This rail should track variations in the DC level of  $MV_{REF}$ .
- Output leakage is measured with all outputs disabled,  $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$ .

Table 14 provides the DDR I/O capacitance when  $GV_{DD}$ (typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for  $GV_{DD}$  (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	$C_{IO}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS	$C_{DIO}$	—	0.5	pF	1

**Note:**

- This parameter is sampled.  $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$ ,  $f = 1 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

Table 15 provides the current draw characteristics for  $MV_{REF}$ .

Table 15. Current Draw Characteristics for  $MV_{REF}$ 

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}$	$I_{MVREF}$	—	500	$\mu A$	1

- The voltage regulator for  $MV_{REF}$  must be able to supply up to 500  $\mu A$  current.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR SDRAM when  $G_{V_{DD}}(\text{typ})=1.8\text{ V}$ .

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	$V_{IL}$	—	$MV_{REF} - 0.25$	V	
AC input high voltage	$V_{IH}$	$MV_{REF} + 0.25$	—	V	

Table 17 provides the input AC timing specifications for the DDR SDRAM when  $G_{V_{DD}}(\text{typ})=2.5\text{ V}$ .

**Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	$V_{IL}$	—	$MV_{REF} - 0.31$	V	
AC input high voltage	$V_{IH}$	$MV_{REF} + 0.31$	—	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 18. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	$t_{CISKEW}$			ps	1, 2
533 MHz		–300	300		
400 MHz		–365	365		
333 MHz		–390	390		

**Note:**

- $t_{CISKEW}$  represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called  $t_{DISKEW}$ . This can be determined by the following equation:  $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$  where T is the clock period and  $\text{abs}(t_{CISKEW})$  is the absolute value of  $t_{CISKEW}$ .

## 6.2.2 DDR SDRAM Output AC Timing Specifications

**Table 19. DDR SDRAM Output AC Timing Specifications**

At recommended operating conditions.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/MCK[n] crossing	$t_{MCK}$	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	$t_{DDKHAS}$			ns	3
533 MHz		1.48	—		
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	$t_{DDKHAX}$			ns	3
533 MHz		1.48	—		
400 MHz		1.95	—		
333 MHz		2.40	—		
MCS[n] output setup with respect to MCK	$t_{DDKHCS}$			ns	3
533 MHz		1.48	—		
400 MHz		1.95	—		
333 MHz		2.40	—		
MCS[n] output hold with respect to MCK	$t_{DDKHGX}$			ns	3
533 MHz		1.48	—		
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	$t_{DDKMHM}$	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	$t_{DDKHDS}$ , $t_{DDKLDS}$			ps	5
533 MHz		538	—		
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	$t_{DDKHDX}$ , $t_{DDKLDX}$			ps	5
533 MHz		538	—		
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	$t_{DDKHMP}$	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

**Table 19. DDR SDRAM Output AC Timing Specifications (continued)**

At recommended operating conditions.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
MDQS epilogue end	$t_{DDKHME}$	-0.6	0.6	ns	6

**Note:**

- The symbols used for timing specifications follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example,  $t_{DDKHAS}$  symbolizes DDR timing (DD) for the time  $t_{MCK}$  memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also,  $t_{DDKLDX}$  symbolizes DDR timing (DD) for the time  $t_{MCK}$  memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{MCK}$  referenced measurements are made from the crossing of the two signals  $\pm 0.1$  V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$ ,  $\overline{MCS}$ , and MDQ/MECC/MDM/MDQS.
- Note that  $t_{DDKHMH}$  follows the symbol conventions described in note 1. For example,  $t_{DDKHMH}$  describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH).  $t_{DDKHMH}$  can be modified through control of the MDQS override bits (called WR\_DATA\_DELAY) in the TIMING\_CFG\_2 register. This will typically be set to the same delay as in DDR\_SDRAM\_CLK\_CNTL[CLK\_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8548E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that  $t_{DDKHMF}$  follows the symbol conventions described in note 1.

**NOTE**

For the ADDR/CMD setup and hold specifications in [Table 19](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 3 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ( $t_{DDKHMH}$ ).

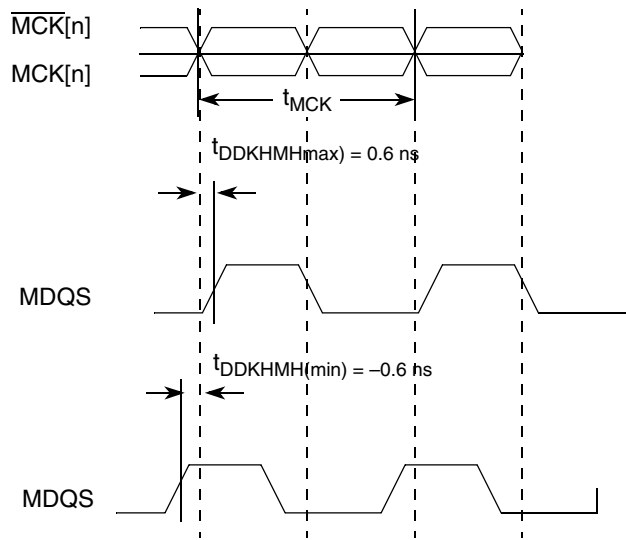


Figure 3. Timing Diagram for  $t_{DDKHMH}$

Figure 4 shows the DDR SDRAM output timing diagram.

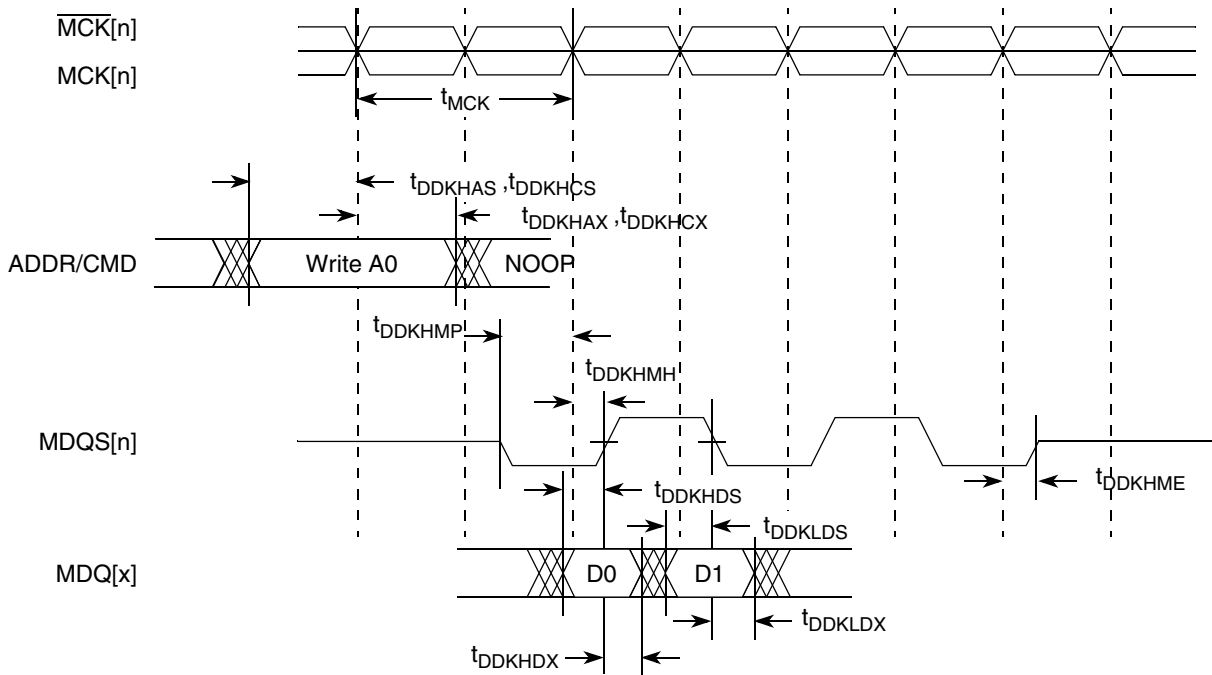


Figure 4. DDR SDRAM Output Timing Diagram



Figure 5 provides the AC test load for the DDR bus.

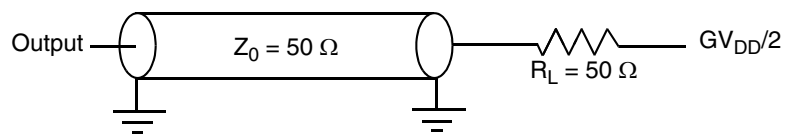


Figure 5. DDR AC Test Load

## 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8548E.

### 7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface.

**Table 20. DUART DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	$V_{IH}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
Input current ( $V_{IN}^1 = 0\text{ V}$ or $V_{IN} = V_{DD}$ )	$I_{IN}$	—	±5	μA
High-level output voltage ( $OV_{DD} = \text{min}$ , $I_{OH} = -2\text{ mA}$ )	$V_{OH}$	2.4	—	V
Low-level output voltage ( $OV_{DD} = \text{min}$ , $I_{OL} = 2\text{ mA}$ )	$V_{OL}$	—	0.4	V

**Note:**

- Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

### 7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface.

**Table 21. DUART AC Timing Specifications**

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB}/1,048,576$	baud	1, 2
Maximum baud rate	$f_{CCB}/16$	baud	1, 2, 3
Oversample rate	16	—	1, 4

**Notes:**

- Guaranteed by design
- $f_{CCB}$  refers to the internal platform clock.
- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8<sup>th</sup> sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.

## 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

### 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V. The GMII, MII, or TBI interface timing is compliant with the IEEE Std. 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

#### 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 22](#) and [Table 23](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 22. GMII, MII, RMII, and TBI DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	$V_{DD}$ $V_{DD}$	3.13	3.47	V	1, 2
Output high voltage ( $V_{DD}/V_{DD} = \text{Min}$ , $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.40	$V_{DD}/V_{DD} + 0.3$	V	
Output low voltage ( $V_{DD}/V_{DD} = \text{Min}$ , $I_{OL} = 4.0 \text{ mA}$ )	$V_{OL}$	GND	0.50	V	
Input high voltage	$V_{IH}$	2.0	$V_{DD}/V_{DD} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	0.90	V	
Input high current ( $V_{IN} = V_{DD}$ , $V_{IN} = V_{DD}$ )	$I_{IH}$	—	40	$\mu\text{A}$	1, 2, 3
Input low current ( $V_{IN} = \text{GND}$ )	$I_{IL}$	-600	—	$\mu\text{A}$	

**Table 22. GMII, MII, RMII, and TBI DC Electrical Characteristics (continued)**

Parameter	Symbol	Min	Max	Unit	Notes
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**Notes:**

1. LV<sub>DD</sub> supports eTSECs 1 and 2.
2. TV<sub>DD</sub> supports eTSECs 3 and 4.
3. The symbol V<sub>IN</sub>, in this case, represents the LV<sub>IN</sub> and TV<sub>IN</sub> symbols referenced in [Table 1](#) and [Table 2](#).

**Table 23. RGMII, RTBI, and FIFO DC Electrical Characteristics**

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV <sub>DD</sub> /TV <sub>DD</sub>	2.37	2.63	V	1, 2
Output high voltage (LV <sub>DD</sub> /TV <sub>DD</sub> = Min, I <sub>OH</sub> = -1.0 mA)	V <sub>OH</sub>	2.00	LV <sub>DD</sub> /TV <sub>DD</sub> + 0.3	V	
Output low voltage (LV <sub>DD</sub> /TV <sub>DD</sub> = Min, I <sub>OL</sub> = 1.0 mA)	V <sub>OL</sub>	GND - 0.3	0.40	V	
Input high voltage	V <sub>IH</sub>	1.70	LV <sub>DD</sub> /TV <sub>DD</sub> + 0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	0.90	V	
Input high current (V <sub>IN</sub> = LV <sub>DD</sub> , V <sub>IN</sub> = TV <sub>DD</sub> )	I <sub>IH</sub>	—	10	μA	1, 2, 3
Input low current (V <sub>IN</sub> = GND)	I <sub>IL</sub>	-15	—	μA	3

**Note:**

1. LV<sub>DD</sub> supports eTSECs 1 and 2.
2. TV<sub>DD</sub> supports eTSECs 3 and 4.
3. Note that the symbol V<sub>IN</sub>, in this case, represents the LV<sub>IN</sub> and TV<sub>IN</sub> symbols referenced in [Table 1](#) and [Table 2](#).

## 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC<sub>n</sub>'s TSEC<sub>n</sub>\_TX\_CLK, while the receive clock must be applied to pin TSEC<sub>n</sub>\_RX\_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out

onto the TSEC<sub>n</sub>\_GTX\_CLK pin (while transmit data appears on TSEC<sub>n</sub>\_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC<sub>n</sub>\_GTX\_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see [Section 4.5, “Platform to FIFO restrictions.”](#)

A summary of the FIFO AC specifications appears in [Table 24](#) and [Table 25](#).

**Table 24. FIFO Mode Transmit AC Timing Specification**

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	$t_{FIT}$	5.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	$t_{FITH}/t_{FIT}$	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	$t_{FITJ}$	—	—	250	ps
Rise time TX_CLK (20%–80%)	$t_{FITR}$	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	$t_{FITF}$	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	$t_{FITDV}$	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	$t_{FITDX}$	0.5	—	3.0	ns

**Table 25. FIFO Mode Receive AC Timing Specification**

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	$t_{FIR}$	5.0	8.0	100	ns
RX_CLK duty cycle	$t_{FIRH}/t_{FIR}$	45	50	55	%
RX_CLK peak-to-peak jitter	$t_{FIRJ}$	—	—	250	ps
Rise time RX_CLK (20%–80%)	$t_{FIRR}$	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	$t_{FIRF}$	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	$t_{FIRDV}$	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	$t_{FIRDV}$	0.5	—	—	ns

Timing diagrams for FIFO appear in Figure 6 and Figure 7.

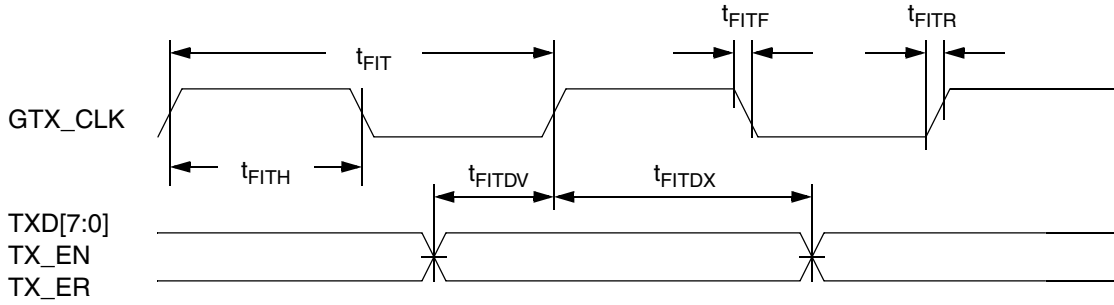


Figure 6. FIFO Transmit AC Timing Diagram

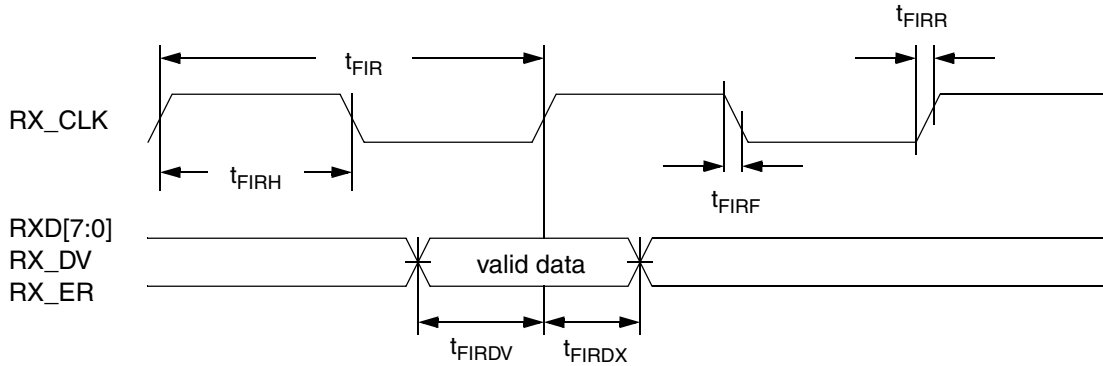


Figure 7. FIFO Receive AC Timing Diagram

## 8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	$t_{GTKHDV}$	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	$t_{GTKHDX}$	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	$t_{GTXR}$ <sup>2</sup>	—	—	1.0	ns

**Table 26. GMII Transmit AC Timing Specifications (continued)**At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
GTX_CLK data clock fall time (80%-20%)	$t_{GTXF}$ <sup>2</sup>	—	—	1.0	ns

**Notes:**

- The symbols used for timing specifications herein follow the pattern  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GTKHVD}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also,  $t_{GTKHDX}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GTX}$  represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design

Figure 8 shows the GMII transmit AC timing diagram.

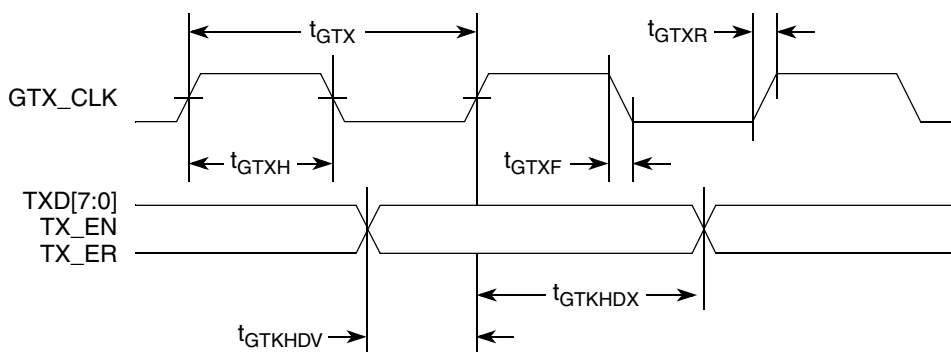
**Figure 8. GMII Transmit AC Timing Diagram****8.2.2.2 GMII Receive AC Timing Specifications**

Table 27 provides the GMII receive AC timing specifications.

**Table 27. GMII Receive AC Timing Specifications**At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RX_CLK clock period	$t_{GRX}$	—	8.0	—	ns
RX_CLK duty cycle	$t_{GRXH}/t_{GRX}$	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	$t_{GRDVKH}$	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	$t_{GRDXKH}$	0	—	—	ns
RX_CLK clock rise (20%-80%)	$t_{GRXR}$ <sup>2</sup>	—	—	1.0	ns

**Table 27. GMII Receive AC Timing Specifications (continued)**

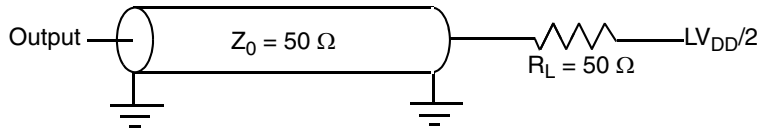
At recommended operating conditions with  $V_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	$t_{GRXF}$ <sup>2</sup>	—	—	1.0	ns

**Note:**

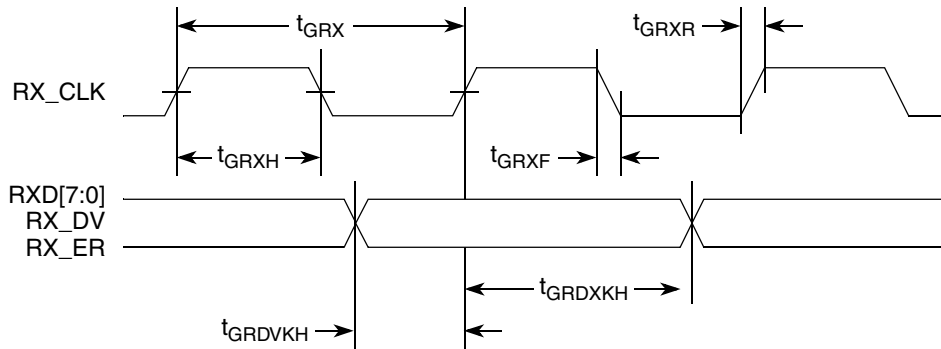
- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GRDVKH}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{RX}$  clock reference (K) going to the high state (H) or setup time. Also,  $t_{GRDXKL}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{GRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GRX}$  represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design

Figure 9 provides the AC test load for eTSEC.



**Figure 9. eTSEC AC Test Load**

Figure 10 shows the GMII receive AC timing diagram.



**Figure 10. GMII Receive AC Timing Diagram**

### 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.



### 8.2.3.1 MII Transmit AC Timing Specifications

Table 28 provides the MII transmit AC timing specifications.

**Table 28. MII Transmit AC Timing Specifications**

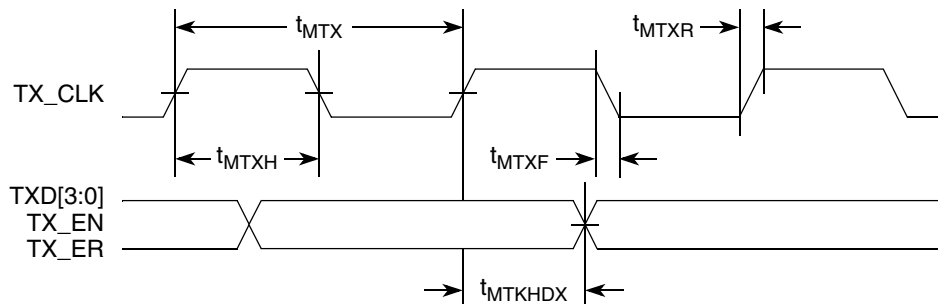
At recommended operating conditions with  $V_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	$t_{MTX}^2$	—	400	—	ns
TX_CLK clock period 100 Mbps	$t_{MTX}$	—	40	—	ns
TX_CLK duty cycle	$t_{MTXH}/t_{MTX}$	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	$t_{MTKHDX}$	1	5	15	ns
TX_CLK data clock rise (20%-80%)	$t_{MTXR}^2$	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	$t_{MTXF}^2$	1.0	—	4.0	ns

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{MTKHDX}$  symbolizes MII transmit timing (MT) for the time  $t_{MTX}$  clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of  $t_{MTX}$  represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 11 shows the MII transmit AC timing diagram.



**Figure 11. MII Transmit AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

Table 29 provides the MII receive AC timing specifications.

**Table 29. MII Receive AC Timing Specifications**

At recommended operating conditions with  $V_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	$t_{MRX}^2$	—	400	—	ns
RX_CLK clock period 100 Mbps	$t_{MRX}$	—	40	—	ns
RX_CLK duty cycle	$t_{MRXH}/t_{MRX}$	35	—	65	%

**Table 29. MII Receive AC Timing Specifications (continued)**

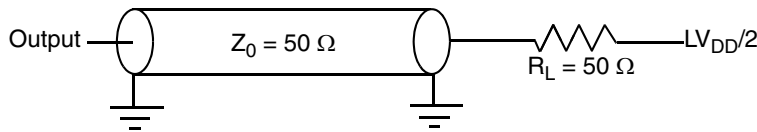
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	$t_{MRDVKH}$	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	$t_{MRDXKH}$	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	$t_{MRXR}^2$	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	$t_{MRXF}^2$	1.0	—	4.0	ns

**Note:**

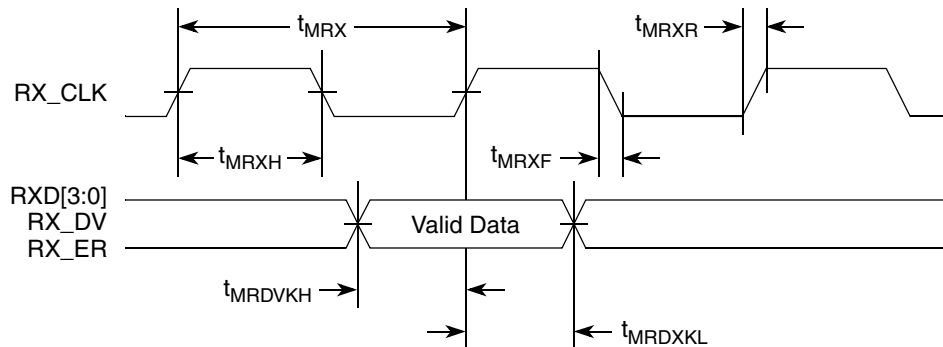
- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MRDVKH}$  symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MRX}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{MRDXKL}$  symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{MRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{MRX}$  represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.



**Figure 12. eTSEC AC Test Load**

Figure 13 shows the MII receive AC timing diagram.



**Figure 13. MII Receive AC Timing Diagram**

### 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 30 provides the TBI transmit AC timing specifications.

**Table 30. TBI Transmit AC Timing Specifications**

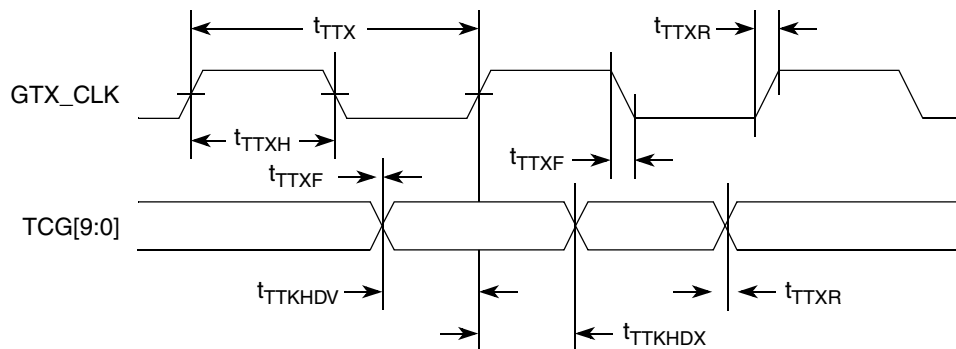
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	$t_{TTKHDV}$	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	$t_{TTKHDX}$	1.0	—	—	ns
GTX_CLK rise (20%–80%)	$t_{TTXR}^2$	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	$t_{TTXF}^2$	—	—	1.0	ns

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{TTKHDV}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also,  $t_{TTKHDX}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{TTX}$  represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 14 shows the TBI transmit AC timing diagram.



**Figure 14. TBI Transmit AC Timing Diagram**

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 31 provides the TBI receive AC timing specifications.

**Table 31. TBI Receive AC Timing Specifications**

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	$t_{TRX}$		16.0		ns
PMA_RX_CLK[0:1] skew	$t_{SKTRX}$	7.5	—	8.5	ns

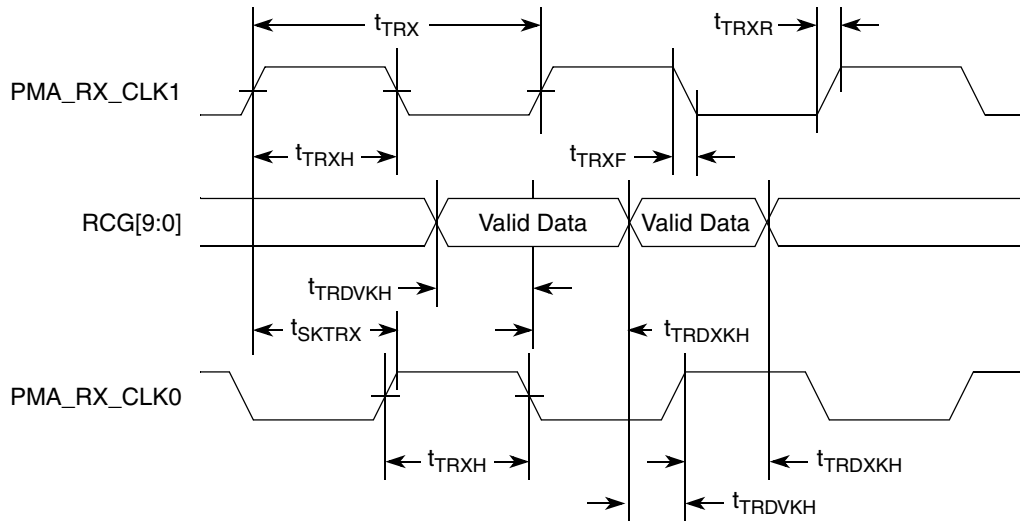
**Table 31. TBI Receive AC Timing Specifications (continued)**

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] duty cycle	$t_{TRXH}/t_{TRX}$	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	$t_{TRDVKH}$	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	$t_{TRDXKH}$	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	$t_{TRXR}^2$	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	$t_{TRXF}^2$	0.7	—	2.4	ns

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{TRDVKH}$  symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{TRX}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{TRDXKH}$  symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{TRX}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{TRX}$  represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

Figure 15 shows the TBI receive AC timing diagram.



**Figure 15. TBI Receive AC Timing Diagram**

### 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC<sub>n</sub>

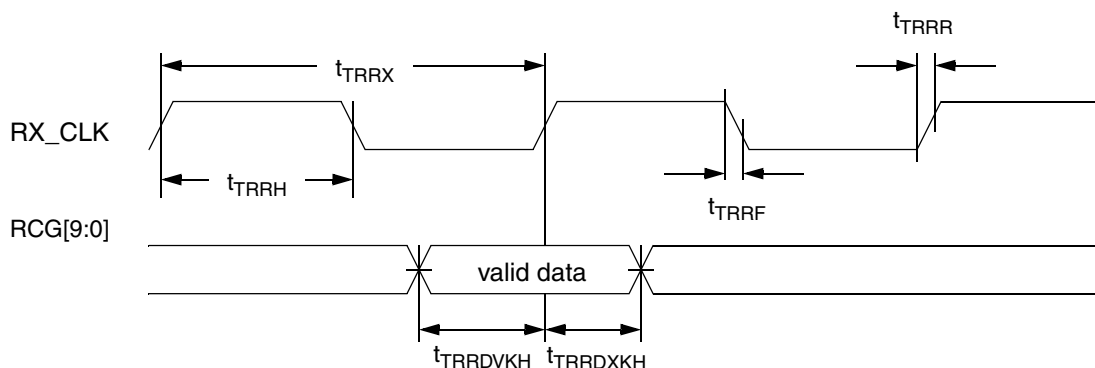
pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in [Table 32](#).

**Table 32. TBI single-clock Mode Receive AC Timing Specification**

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	$t_{TRRX}$	7.5	8.0	8.5	ns
RX_CLK duty cycle	$t_{TRRH}/t_{TRRX}$	40	50	60	%
RX_CLK peak-to-peak jitter	$t_{TRRJ}$	—	—	250	ps
Rise time RX_CLK (20%–80%)	$t_{TRRR}$	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	$t_{TRRF}$	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDVKH}$	1.0	—	—	ns

A timing diagram for TBI receive appears in [Figure 16](#).



**Figure 16. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.2.6 RGMII and RTBI AC Timing Specifications

[Table 33](#) presents the RGMII and RTBI AC timing specifications.

**Table 33. RGMII and RTBI AC Timing Specifications**

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	$t_{SKRGT}$ <sup>5</sup>	-500 <sup>6</sup>	0	500 <sup>6</sup>	ps
Data to clock input skew (at receiver) <sup>2</sup>	$t_{SKRGT}$	1.0	—	2.8	ns
Clock period <sup>3</sup>	$t_{RGT}$ <sup>5</sup>	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 4</sup>	$t_{RGTH}/t_{RGT}$ <sup>5</sup>	40	50	60	%
Rise time (20%–80%)	$t_{RGTR}$ <sup>5</sup>	—	—	0.75	ns

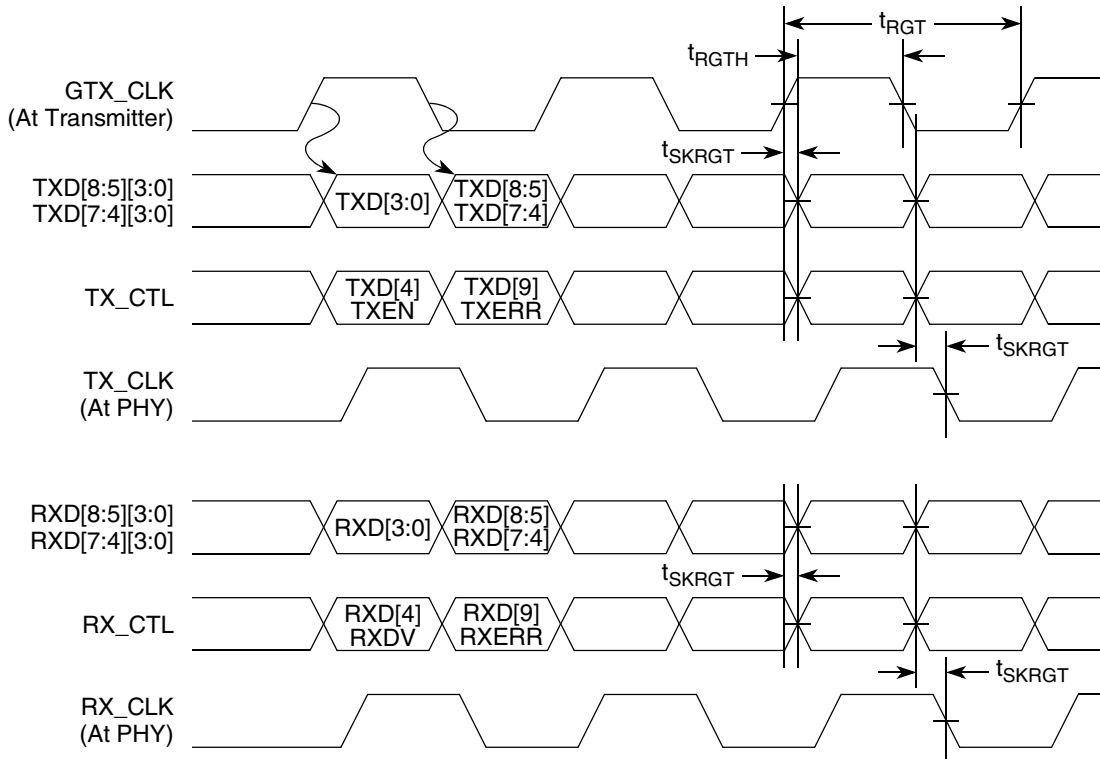
**Table 33. RGMII and RTBI AC Timing Specifications**

Fall time (20%–80%)	$t_{\text{RGT}}^5$	—	—	0.75	ns
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**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of  $t_{\text{RGT}}$  represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps,  $t_{\text{RGT}}$  scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{\text{RGT}}$  of the lowest speed transitioned between.
5. Guaranteed by characterization
6. In rev 1.0 silicon, due to errata,  $t_{\text{SKRGT}}$  is -650 ps (Min) and 650 ps (Max). Please refer to “eTSEC 10” in the device errata document.

Figure 17 shows the RGMII and RTBI AC timing and multiplexing diagrams.



**Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams**

### 8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in [Table 34](#).

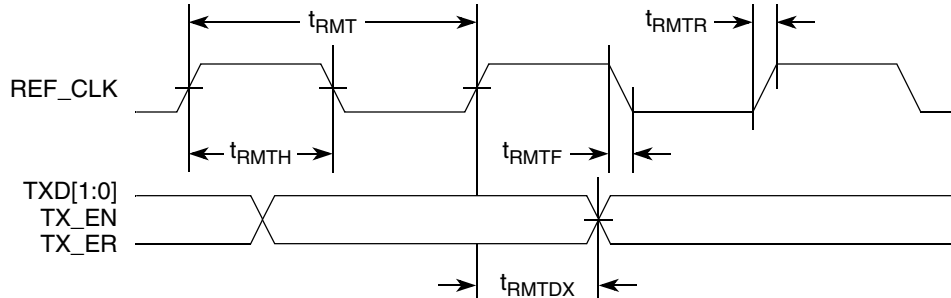
**Table 34. RMII Transmit AC Timing Specifications**

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
REF_CLK clock period	$t_{RMT}$	15.0	20.0	25.0	ns
REF_CLK duty cycle	$t_{RMTH}$	35	50	65	%
REF_CLK peak-to-peak jitter	$t_{RMTJ}$	—	—	250	ps
Rise time REF_CLK (20%–80%)	$t_{RMTR}$	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	$t_{RMTF}$	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTDX}$	1.0	—	10.0	ns

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{MTKHDX}$  symbolizes MII transmit timing (MT) for the time  $t_{MTX}$  clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of  $t_{MTX}$  represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[Figure 18](#) shows the RMII transmit AC timing diagram.



**Figure 18. RMII Transmit AC Timing Diagram**

### 8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
REF_CLK clock period	$t_{RMR}$	15.0	20.0	25.0	ns
REF_CLK duty cycle	$t_{RMRH}$	35	50	65	%
REF_CLK peak-to-peak jitter	$t_{RMRJ}$	—	—	250	ps
Rise time REF_CLK (20%–80%)	$t_{RMRR}$	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	$t_{RMRF}$	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	$t_{RMRDV}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	$t_{RMRDX}$	2.0	—	—	ns

**Note:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MRDVKH}$  symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MRX}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{MRDXKL}$  symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{MRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{MRX}$  represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 provides the AC test load for eTSEC.

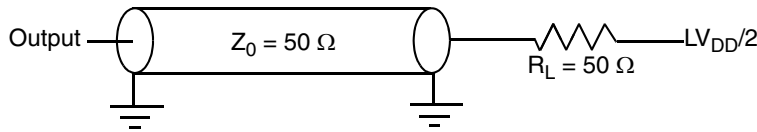


Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.

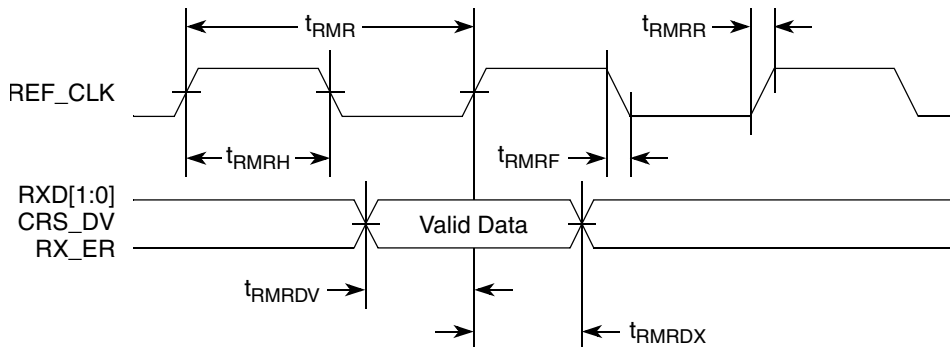


Figure 20. RMII Receive AC Timing Diagram



## 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in “[Section 8, “Ethernet: Enhanced Three-Speed Ethernet \(eTSEC\), MII Management.”](#)”

### 9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 36](#).

**Table 36. MII Management DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	$OV_{DD}$	3.13	3.47	V
Output high voltage ( $OV_{DD} = \text{Min}$ , $I_{OH} = -1.0 \text{ mA}$ )	$V_{OH}$	2.10	$OV_{DD} + 0.3$	V
Output low voltage ( $OV_{DD} = \text{Min}$ , $I_{OL} = 1.0 \text{ mA}$ )	$V_{OL}$	GND	0.50	V
Input high voltage	$V_{IH}$	2.0	—	V
Input low voltage	$V_{IL}$	—	0.90	V
Input high current ( $OV_{DD} = \text{Max}$ , $V_{IN}^1 = 2.1 \text{ V}$ )	$I_{IH}$	—	40	$\mu\text{A}$
Input low current ( $OV_{DD} = \text{Max}$ , $V_{IN} = 0.5 \text{ V}$ )	$I_{IL}$	-600	—	$\mu\text{A}$

**Note:**

- Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

### 9.2 MII Management AC Electrical Specifications

[Table 37](#) provides the MII management AC timing specifications.

**Table 37. MII Management AC Timing Specifications**

At recommended operating conditions with  $OV_{DD}$  is 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Max	Unit	Notes
MDC frequency	$f_{MDC}$	5.2	8.3	MHz	2, 4
MDC period	$t_{MDC}$	120	192	ns	
MDC clock pulse width high	$t_{MDCH}$	32	—	ns	
MDC to MDIO valid	$t_{MDKHDV}$	$16 \cdot t_{CCB}$		ns	5
MDC to MDIO delay	$t_{MDKHDX}$	10	$16 \cdot t_{CCB}$	ns	3, 5

**Table 37. MII Management AC Timing Specifications (continued)**

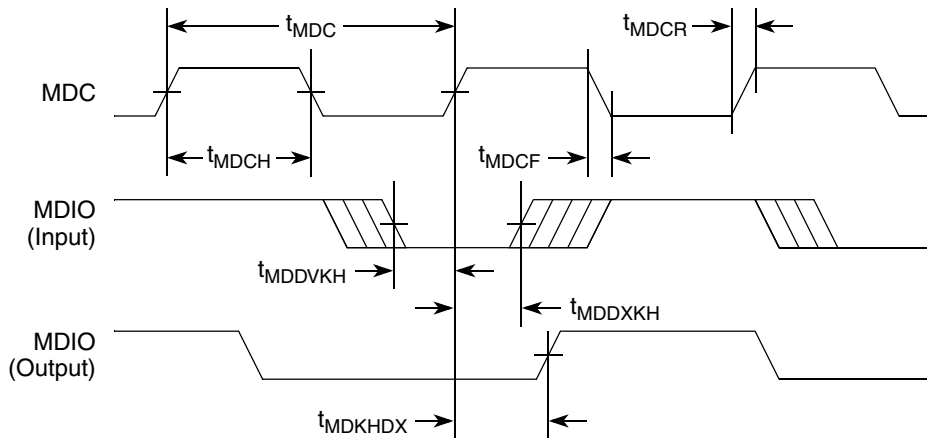
At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Max	Unit	Notes
MDIO to MDC setup time	$t_{MDDVKH}$	5	—	ns	
MDIO to MDC hold time	$t_{MDDXKH}$	0	—	ns	
MDC rise time	$t_{MDCR}$	—	10	ns	4
MDC fall time	$t_{MDHF}$	—	10	ns	4

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MDKHDX}$  symbolizes management data timing (MD) for the time  $t_{MDC}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{MDDVKH}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MDC}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design
5.  $t_{CCB}$  is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



**Figure 21. MII Management Interface Timing Diagram**

## 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8548E.

### 10.1 Local Bus DC Electrical Characteristics

[Table 38](#) provides the DC electrical characteristics for the local bus interface operating at  $BV_{DD} = 3.3$  V DC.

**Table 38. Local Bus DC Electrical Characteristics (3.3 V DC)**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	$V_{IH}$	2	$BV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
Input current ( $V_{IN}^1 = 0$ V or $V_{IN} = BV_{DD}$ )	$I_{IN}$	—	$\pm 5$	$\mu$ A
High-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OH} = -2$ mA)	$V_{OH}$	2.4	—	V
Low-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OL} = 2$ mA)	$V_{OL}$	—	0.4	V

**Note:**

- Note that the symbol  $V_{IN}$ , in this case, represents the  $BV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

[Table 39](#) provides the DC electrical characteristics for the local bus interface operating at  $BV_{DD} = 2.5$  V DC.

**Table 39. Local Bus DC Electrical Characteristics (2.5 V DC)**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	$V_{IH}$	1.70	$BV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.7	V
Input current ( $V_{IN}^1 = 0$ V or $V_{IN} = BV_{DD}$ )	$I_{IH}$	—	10	$\mu$ A
	$I_{IL}$		-15	
High-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OH} = -1$ mA)	$V_{OH}$	2.0	—	V
Low-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OL} = 1$ mA)	$V_{OL}$	—	0.4	V

**Note:**

- Note that the symbol  $V_{IN}$ , in this case, represents the  $BV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

## 10.2 Local Bus AC Electrical Specifications

Table 40 describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V. For information about the frequency range of local bus see Section 19.1, “Clock Ranges.”

**Table 40. Local Bus Timing Parameters ( $BV_{DD} = 3.3$  V)—PLL Enabled**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	$t_{LBK}$	7.5	12	ns	2
Local bus duty cycle	$t_{LBKH}/t_{LBK}$	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	$t_{LBOTOT}$	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5

**Table 40. Local Bus Timing Parameters (BV<sub>DD</sub> = 3.3 V)—PLL Enabled (continued)**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>	—	2.5	ns	5

**Note:**

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(First two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one(1). Also, t<sub>LBKHOX</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- All signals are measured from BV<sub>DD</sub>/2 of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV<sub>DD</sub> of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- Guaranteed by design.

Table 41 describes the timing parameters of the local bus interface at BV<sub>DD</sub> = 2.5 V.

**Table 41. Local Bus Timing Parameters (BV<sub>DD</sub> = 2.5 V)—PLL Enabled**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	12	ns	2
Local bus duty cycle	t <sub>LBKH</sub> /t <sub>LBK</sub>	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/UPWAIT)	t <sub>LBIVKH1</sub>	1.9	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.8	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.1	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.1	ns	
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.3	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.4	ns	3

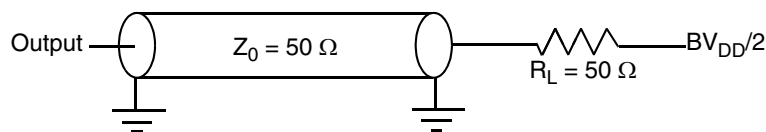
**Table 41. Local Bus Timing Parameters ( $BV_{DD} = 2.5\text{ V}$ )—PLL Enabled (continued)**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{LBIXKH1}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{LBK}$  clock reference (K) goes high (H), in this case for clock one(1). Also,  $t_{LBKHOX}$  symbolizes local bus timing (LB) for the  $t_{LBK}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- $t_{LBOTOT}$  is a measurement of the minimum time between the negation of LALE and any change in LAD.  $t_{LBOTOT}$  is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at  $BV_{DD}/2$ .
- Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

**Figure 22. Local Bus AC Test Load****NOTE**

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 Mhz, LBIU PLL is recommended to be enabled.

Figure 23 to Figure 28 show the local bus signals.

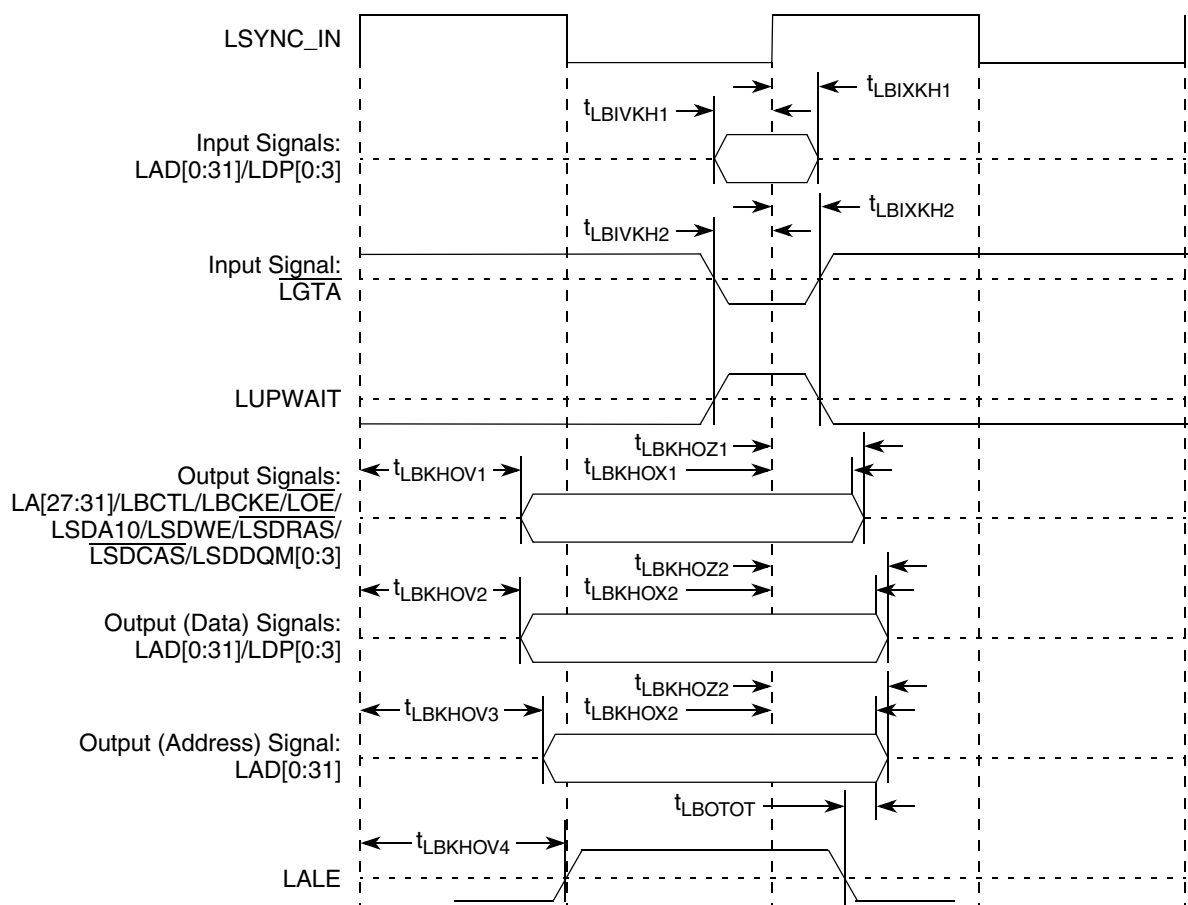


Figure 23. Local Bus Signals (PLL Enabled)

Table 42 describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3\text{ V}$  with PLL disabled.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	$t_{LBK}$	12	—	ns	2
Local bus duty cycle	$t_{LBKH}/t_{LBK}$	43	57	%	
Internal launch/capture clock to LCLK delay	$t_{LBKHKT}$	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIXKH1}$	-1.8	—	ns	4, 5
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKL2}$	-1.3	—	ns	4, 5

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
LALE output transition to LAD/LDP output transition (LATCH hold time)	$t_{LBOTOT}$	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	-0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	-0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

## Notes:

- The symbols used for timing specifications herein follow the pattern of  $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{LBIXKH1}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{LBK}$  clock reference (K) goes high (H), in this case for clock one(1). Also,  $t_{LBKHGX}$  symbolizes local bus timing (LB) for the  $t_{LBK}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by  $t_{LBKHK1}$ .
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at  $BV_{DD}/2$ .
- All signals are measured from  $BV_{DD}/2$  of the rising edge of local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- The value of  $t_{LBOTOT}$  is the measurement of the minimum time between the negation of LALE and any change in LAD.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Guaranteed by characterization.
- Guaranteed by design.



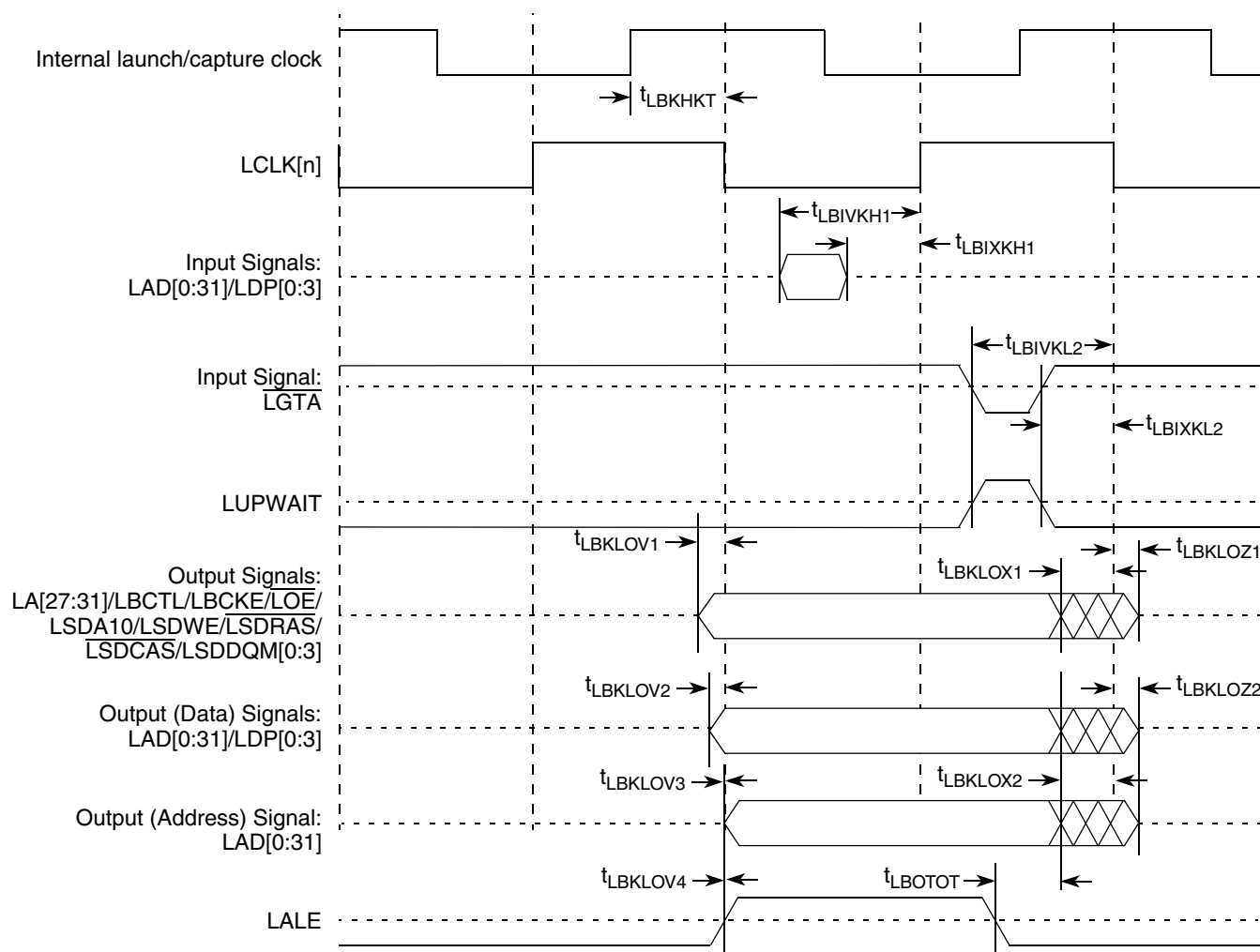


Figure 24. Local Bus Signals (PLL Bypass Mode)

#### NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of  $t_{LBKHKHT}$ . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).

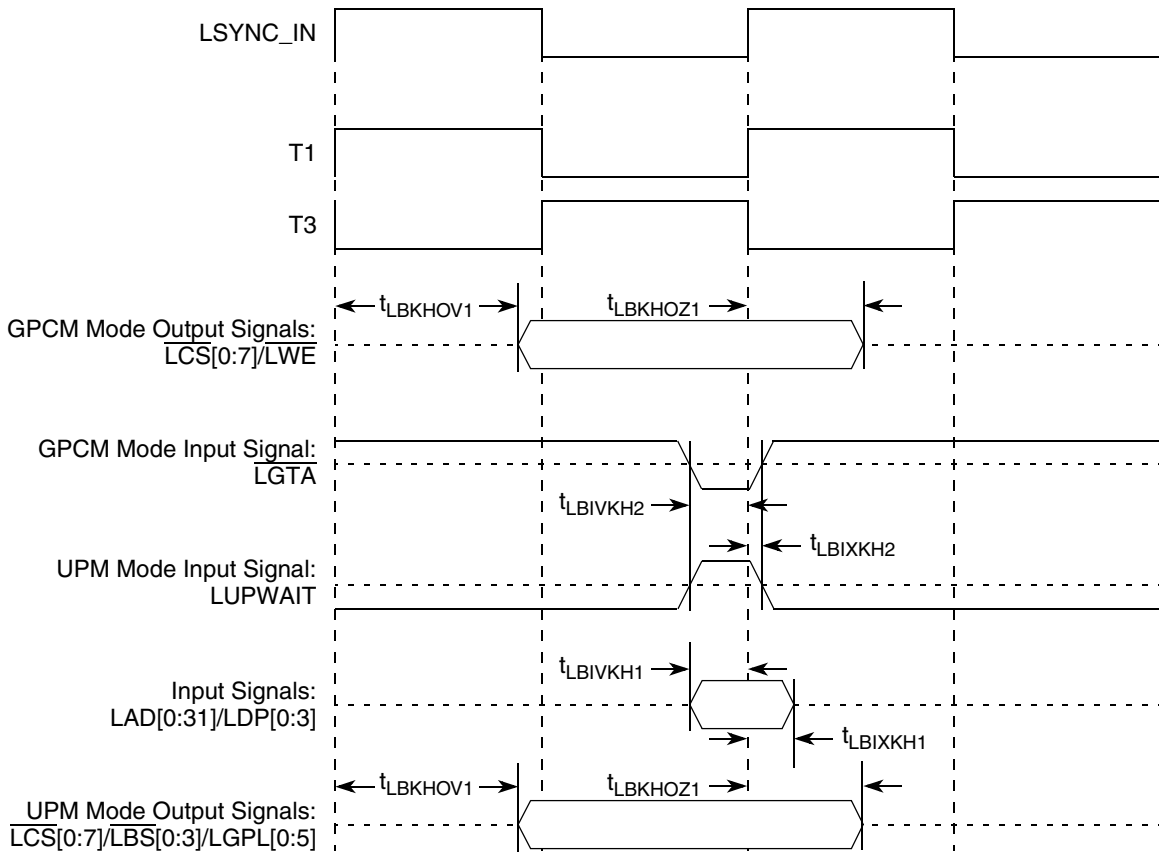


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

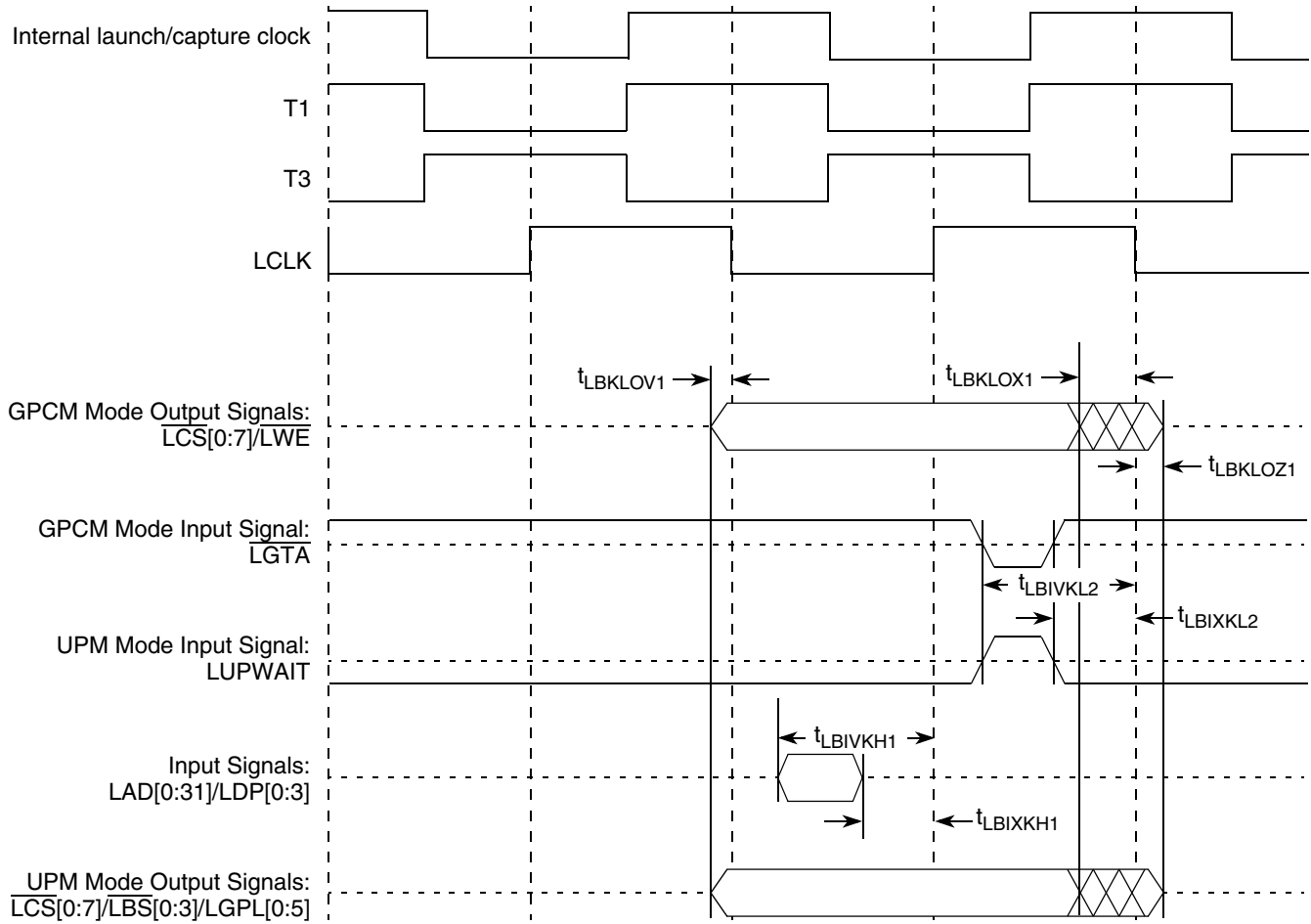


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

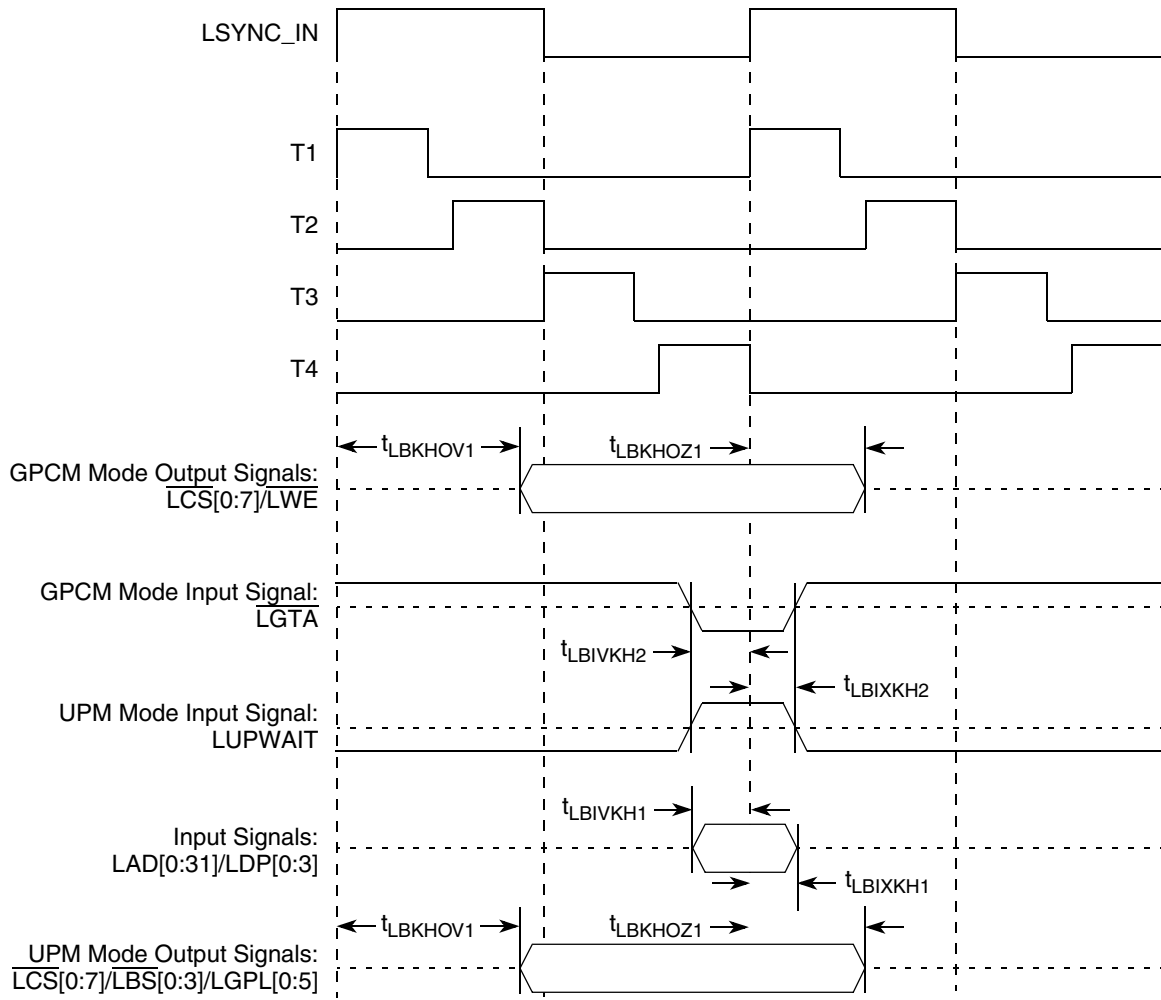


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

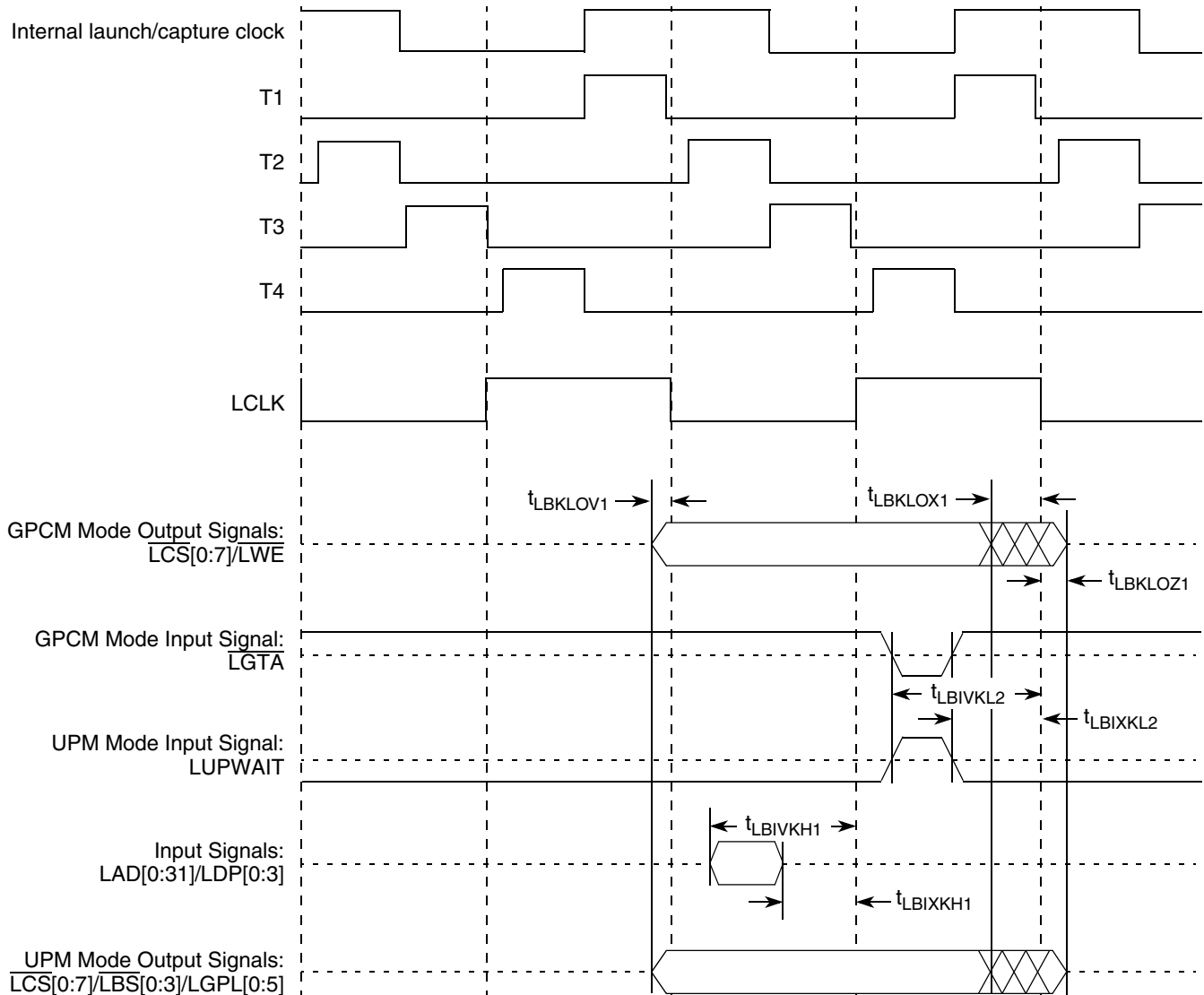


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

## 11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

## 12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8548E.

### 12.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol <sup>1</sup>	Min	Max	Unit
High-level input voltage	$V_{IH}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
Input current ( $V_{IN}^1 = 0$ V or $V_{IN} = V_{DD}$ )	$I_{IN}$	—	$\pm 5$	$\mu$ A
High-level output voltage ( $OV_{DD} = \text{min}$ , $I_{OH} = -2$ mA)	$V_{OH}$	2.4	—	V
Low-level output voltage ( $OV_{DD} = \text{min}$ , $I_{OL} = 2$ mA)	$V_{OL}$	—	0.4	V

**Notes:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$ .

### 12.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 30 through Figure 32.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)<sup>1</sup>

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	$f_{JTG}$	0	33.3	MHz	
JTAG external clock cycle time	$t_{JTG}$	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	$t_{JTKHKL}$	15	—	ns	
JTAG external clock rise and fall times	$t_{JTGR}$ & $t_{JTGF}$	0	2	ns	6
$\overline{\text{TRST}}$ assert time	$t_{TRST}$	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	$t_{JTDVKH}$ $t_{JTIVKH}$	4 0	— —	ns	4
Input hold times: Boundary-scan data TMS, TDI	$t_{JTDXKH}$ $t_{JTIXKH}$	20 25	— —	ns	4

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) <sup>1</sup> (continued)**

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	$t_{JTKLDV}$ $t_{JTKLOV}$	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	$t_{JTKLDX}$ $t_{JTKLOX}$	30 30	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	$t_{JTKLDZ}$ $t_{JTKLOZ}$	3 3	19 9	ns	5, 6

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{JTDVKH}$  symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTDXKH}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3.  $\overline{TRST}$  is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to  $t_{TCLK}$ .
5. Non-JTAG signal output timing with respect to  $t_{TCLK}$ .
6. Guaranteed by design

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.

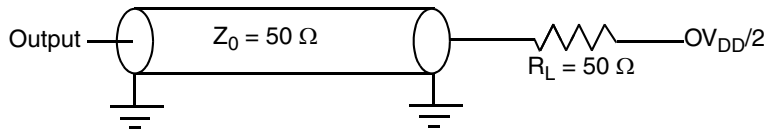


Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.

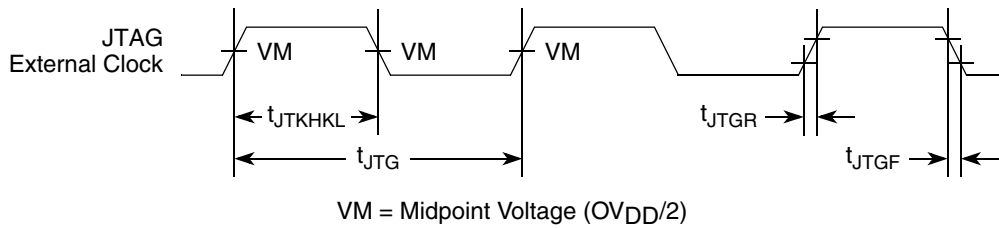


Figure 30. JTAG Clock Input Timing Diagram

Figure 31 provides the  $\overline{\text{TRST}}$  timing diagram.

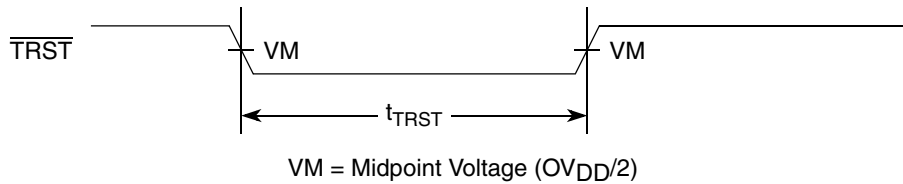


Figure 31.  $\overline{\text{TRST}}$  Timing Diagram

Figure 32 provides the boundary-scan timing diagram.

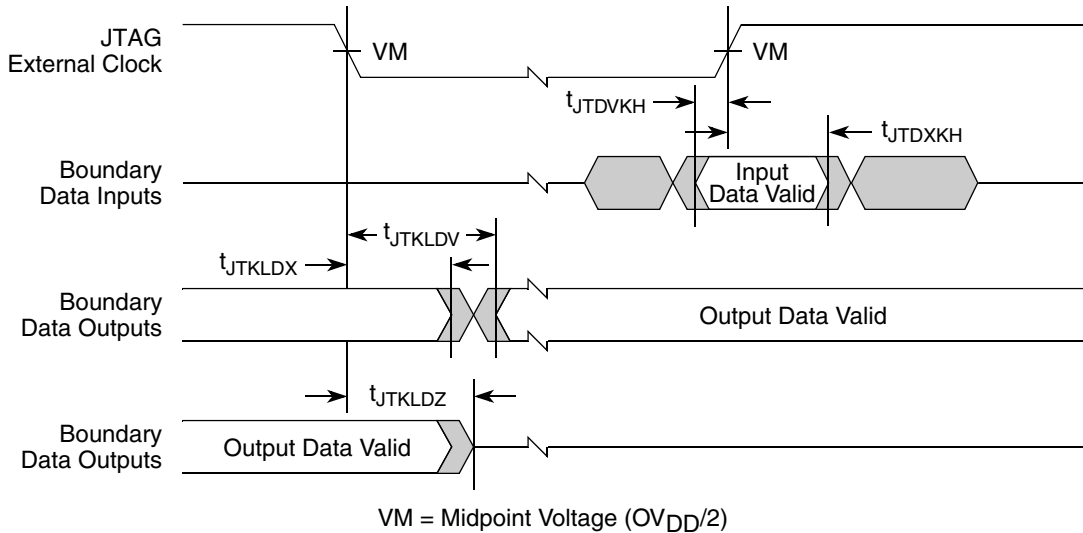


Figure 32. Boundary-Scan Timing Diagram



## 13 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the I<sup>2</sup>C interfaces of the MPC8548E.

### 13.1 I<sup>2</sup>C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I<sup>2</sup>C interfaces.

**Table 45. I<sup>2</sup>C DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V <sub>IH</sub>	0.7 × OV <sub>DD</sub>	OV <sub>DD</sub> + 0.3	V	
Input low voltage level	V <sub>IL</sub>	−0.3	0.3 × OV <sub>DD</sub>	V	
Low level output voltage	V <sub>OL</sub>	0	0.2 × OV <sub>DD</sub>	V	1
Pulse width of spikes which must be suppressed by the input filter	t <sub>12KHKL</sub>	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 × OV <sub>DD</sub> and 0.9 × OV <sub>DD</sub> (max))	I <sub>I</sub>	−10	10	μA	3
Capacitance for each I/O pin	C <sub>I</sub>	—	10	pF	

**Notes:**

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8548E PowerQUICC III Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV<sub>DD</sub> is switched off.

## 13.2 I<sup>2</sup>C AC Electrical Specifications

Table 46 provides the AC timing parameters for the I<sup>2</sup>C interfaces.

**Table 46. I<sup>2</sup>C AC Electrical Specifications**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
SCL clock frequency	f <sub>I2C</sub>	0	400	kHz	
Low period of the SCL clock	t <sub>I2CL</sub>	1.3	—	μs	4
High period of the SCL clock	t <sub>I2CH</sub>	0.6	—	μs	4
Setup time for a repeated START condition	t <sub>I2SVKH</sub>	0.6	—	μs	4
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t <sub>I2SXKL</sub>	0.6	—	μs	4
Data setup time	t <sub>I2DVKH</sub>	100	—	ns	4
Data input hold time: CBUS compatible masters I <sup>2</sup> C bus devices	t <sub>I2DXKL</sub>	— 0	— —	μs	2
Data output delay time:	t <sub>I2OVKL</sub>	—	0.9		3
Set-up time for STOP condition	t <sub>I2PVKH</sub>	0.6	—	μs	
Bus free time between a STOP and START condition	t <sub>I2KHDX</sub>	1.3	—	μs	
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	0.1 × OV <sub>DD</sub>	—	V	

Table 46. I<sup>2</sup>C AC Electrical Specifications (continued)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Noise margin at the HIGH level for each connected device (including hysteresis)	$V_{NH}$	$0.2 \times OV_{DD}$	—	V	

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{I2DVKH}$  symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{I2SXKL}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the  $t_{I2C}$  clock reference (K) going to the low (L) state or hold time. Also,  $t_{I2PVKH}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- As a transmitter, the MPC8548E provides a delay time of at least 300 ns for the SDA signal (refer to the  $V_{IH(min)}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When MPC8548E acts as the I<sup>2</sup>C bus master while transmitting, MPC8548E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, MPC8548E would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for MPC8548E as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I<sup>2</sup>C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I<sup>2</sup>C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I <sup>2</sup> C Source Clock Frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR Bit Setting	0x2A	0x05	0x26	0x00
Actual FDR Divider Selected	896	704	512	384
Actual I <sup>2</sup> C SCL Frequency Generated	371 kHz	378 kHz	390 kHz	346 kHz

For the detail of I<sup>2</sup>C frequency calculation, refer to the application note AN2919 “Determining the I<sup>2</sup>C Frequency Divider Ratio for SCL”. Note that the I<sup>2</sup>C Source Clock Frequency is half of the CCB clock frequency for MPC8548E.
- The maximum  $t_{I2DXKL}$  has only to be met if the device does not stretch the LOW period ( $t_{I2CL}$ ) of the SCL signal.
- Guaranteed by design

Figure 29 provides the AC test load for the I<sup>2</sup>C.

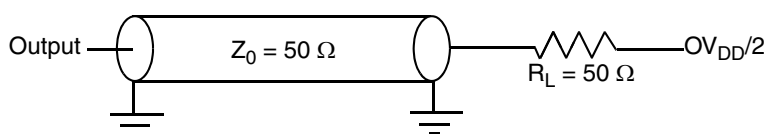
Figure 33. I<sup>2</sup>C AC Test Load

Figure 34 shows the AC timing diagram for the I<sup>2</sup>C bus.

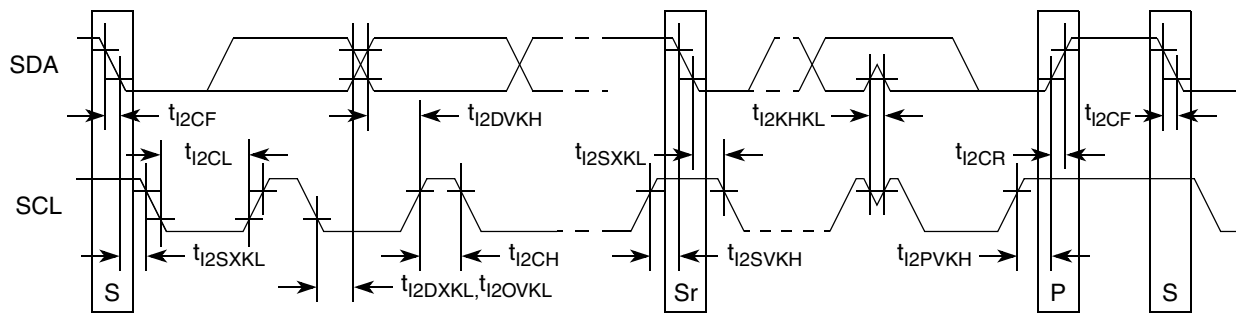


Figure 34. I<sup>2</sup>C Bus AC Timing Diagram

## 14 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8548E. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

### 14.1 PCI/PCI-X DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 47. PCI/PCI-X DC Electrical Characteristics <sup>1</sup>

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V	
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V	
Input current (V <sub>IN</sub> = 0 V or V <sub>IN</sub> = V <sub>DD</sub> )	I <sub>IN</sub>	—	±5	μA	2
High-level output voltage (OV <sub>DD</sub> = min, I <sub>OH</sub> = -2 mA)	V <sub>OH</sub>	2.4	—	V	
Low-level output voltage (OV <sub>DD</sub> = min, I <sub>OL</sub> = 2 mA)	V <sub>OL</sub>	—	0.4	V	

**Notes:**

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V<sub>IN</sub>, in this case, represents the OV<sub>IN</sub> symbol referenced in [Table 1](#) and [Table 2](#).

### 14.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for asynchronous mode and by PCIn\_CLK when it is configured for asynchronous mode.

Table 48 provides the PCI AC timing specifications at 66 MHz.

Table 48. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
CLK to output valid	$t_{PCKHOV}$	—	6.0	ns	2, 3
Output hold from CLK	$t_{PCKHOX}$	2.0	—	ns	2, 10
CLK to output high impedance	$t_{PCKHOZ}$	—	14	ns	2, 4, 11
Input setup to CLK	$t_{PCIVKH}$	3.0	—	ns	2, 5, 10
Input hold from CLK	$t_{PCIXKH}$	0	—	ns	2, 5, 10
$\overline{REQ64}$ to $\overline{HRESET}$ <sup>9</sup> setup time	$t_{PCRVRH}$	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	$t_{PCRHRX}$	0	50	ns	7, 11
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	$t_{PCRHFV}$	10	—	clocks	8, 11

Notes:

- Note that the symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{PCIVKH}$  symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock,  $t_{SYS}$ , reference (K) going to the high (H) state or setup time. Also,  $t_{PCRHFV}$  symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- All PCI signals are measured from  $OV_{DD}/2$  of the rising edge of SYSCLK or PCI\_CLK $n$  to  $0.4 \times OV_{DD}$  of the signal in question for 3.3-V PCI signaling levels.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter  $t_{SYS}$  indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see [Section 19, "Clocking."](#)
- The setup and hold time is with respect to the rising edge of  $\overline{HRESET}$ .
- The timing parameter  $t_{PCRHFV}$  is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for  $\overline{HRESET}$  is 100  $\mu\text{s}$ .
- Guaranteed by characterization
- Guaranteed by design

Figure 35 provides the AC test load for PCI and PCI-X.

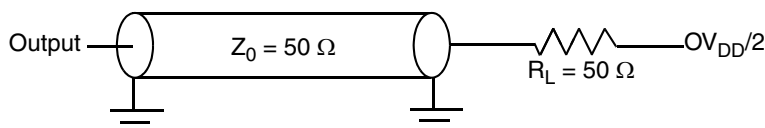


Figure 35. PCI/PCI-X AC Test Load

Figure 36 shows the PCI/PCI-X input AC timing conditions.

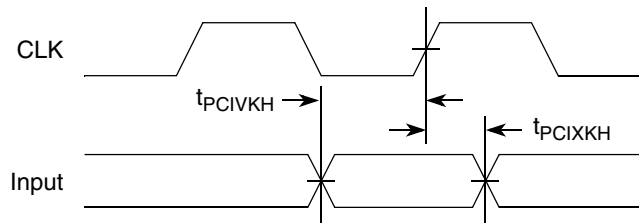


Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.

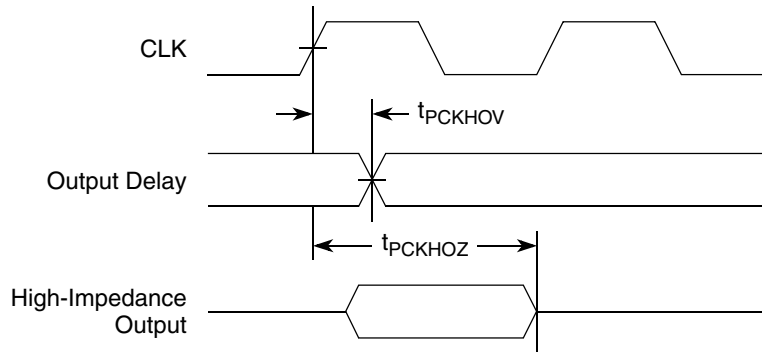


Figure 37. PCI/PCI-X Output AC Timing Measurement Condition

Table 49 provides the PCI-X AC timing specifications at 66 MHz.

Table 49. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	$t_{PCKHOV}$	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	$t_{PCKHOX}$	0.7	—	ns	1, 10
SYSCLK to output high impedance	$t_{PCKHOZ}$	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	$t_{PCIVKH}$	1.7	—	ns	3, 5
Input hold time from SYSCLK	$t_{PCIXKH}$	0.5	—	ns	10
$\overline{REQ64}$ to $\overline{HRESET}$ setup time	$t_{PCRVRH}$	10	—	clocks	11
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	$t_{PCRHRX}$	0	50	ns	11
$\overline{HRESET}$ high to first FRAME assertion	$t_{PCRHFV}$	10	—	clocks	9, 11
PCI-X initialization pattern to $\overline{HRESET}$ setup time	$t_{PCIVRH}$	10	—	clocks	11

Table 49. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	$t_{\text{PCRHI X}}$	0	50	ns	6, 11

**Notes:**

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to  $\overline{\text{REQ}}$  and  $\overline{\text{GNT}}$  only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for  $\overline{\text{HRESET}}$  high to first configuration access,  $t_{\text{PCRHFV}}$ ). The PCI-X initialization pattern control signals after the rising edge of  $\overline{\text{HRESET}}$  must be negated no later than two clocks before the first  $\overline{\text{FRAME}}$  and must be floated no later than one clock before  $\overline{\text{FRAME}}$  is asserted.
7. A PCI-X device is permitted to have the minimum values shown for  $t_{\text{PCKHOV}}$  and  $t_{\text{CYC}}$  only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter  $t_{\text{PCRHFV}}$  is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.
10. Guaranteed by characterization
11. Guaranteed by design

Table 50 provides the PCI-X AC timing specifications at 133 MHz.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Table 50. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	$t_{\text{PCKHOV}}$	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	$t_{\text{PCKHOX}}$	0.7	—	ns	1, 11
SYSCLK to output high impedance	$t_{\text{PCKHOZ}}$	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	$t_{\text{PCIVKH}}$	1.2	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	$t_{\text{PCIXKH}}$	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	$t_{\text{PCRVRH}}$	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	$t_{\text{PCRHRX}}$	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	$t_{\text{PCRHFV}}$	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	$t_{\text{PCIVRH}}$	10	—	clocks	12

Table 50. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	$t_{\text{PCRHX}}$	0	50	ns	6, 12

**Notes:**

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to  $\overline{\text{REQ}}$  and  $\overline{\text{GNT}}$  only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for  $\overline{\text{HRESET}}$  high to first configuration access,  $t_{\text{PCRHFV}}$ ). The PCI-X initialization pattern control signals after the rising edge of  $\overline{\text{HRESET}}$  must be negated no later than two clocks before the first  $\overline{\text{FRAME}}$  and must be floated no later than one clock before  $\overline{\text{FRAME}}$  is asserted.
7. A PCI-X device is permitted to have the minimum values shown for  $t_{\text{PCKHOV}}$  and  $t_{\text{CYC}}$  only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter  $t_{\text{PCIVKH}}$  is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification*.
10. The timing parameter  $t_{\text{PCRHFV}}$  is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.
11. Guaranteed by characterization
11. Guaranteed by design



## 15 High-Speed Interfaces

This section describes the common specifications for the high-speed interconnect interfaces (Serial RapidIO and PCI Express) of the MPC8548E.

### 15.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks are  $\overline{\text{SD\_REF\_CLK}}$  and  $\overline{\text{SD\_REF\_CLK}}$ .

- Each differential clock input has an internal  $50\text{-}\Omega$  termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled on chip following the termination.
- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak. Each single wire of the differential pair must have a single-ended swing less than 800 mV and an average voltage between 0 and 400mV.
- The differential reference clock ( $\overline{\text{SD\_REF\_CLK}}/\overline{\text{SD\_REF\_CLK}}$ ) input is HCSL compatible DC coupled or LVDS compatible with AC coupling.

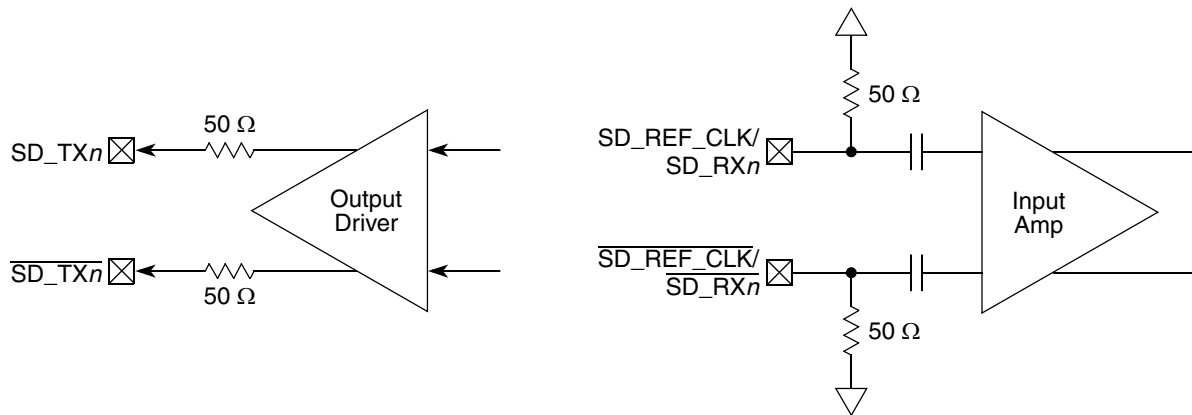


Figure 38. Driver and Receiver of SerDes (PCI Express, Serial RapidIO, and  $\overline{\text{SD\_REF\_CLK}}/\overline{\text{SD\_REF\_CLK}}$ )

### 15.2 Spread Spectrum Clock

$\overline{\text{SD\_REF\_CLK}}/\overline{\text{SD\_REF\_CLK}}$  was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

## 16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

### 16.1 DC Requirements for PCI Express SD\_REF\_CLK and SD\_REF\_CLK

For more information, see [Section 15.1, “DC Requirements for SerDes Reference Clocks.”](#)

### 16.2 AC Requirements for PCI Express SerDes Clocks

[Table 51](#) lists AC requirements.

**Table 51. SD\_REF\_CLK and SD\_REF\_CLK AC Requirements**

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
$t_{REF}$	REFCLK cycle time	-	10	-	ns	1
$t_{REFCJ}$	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
$t_{REFPJ}$	Phase jitter. Deviation in edge location with respect to mean edge location	-50	—	50	ps	—

Notes:

1. Typical based on PCI Express Specification 2.0.

### 16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/- 300 ppm tolerance.

### 16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

## 16.4.1 Differential Transmitter (TX) Output

Table 52 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 52. Differential Transmitter (TX) Output Specifications**

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2 *  V_{TX-D+} - V_{TX-D-} $ See Note 2.
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
$T_{TX-EYE}$	Minimum TX Eye Width	0.70			UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = \text{RMS}( V_{TXD+} - V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During LO and Electrical Idle	0		100	mV	$ V_{TX-CM-DC}(\text{during LO}) - V_{TX-CM-Idle-DC}(\text{During Electrical Idle})  \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D-	0		25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}  \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $ V_{TX-D-} $ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} =  V_{TX-IDLE-D+} - V_{TX-IDLE-D-}  \leq 20$ mV See Note 2.

Table 52. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0		3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit			90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set			20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from LO.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$RL_{TX-CM}$	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	$\Omega$	TX DC Differential mode Low Impedance
$Z_{TX-DC}$	Transmitter DC Impedance	40			$\Omega$	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
$C_{TX}$	AC Coupling Capacitor	75		200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 52. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{\text{crosslink}}$	Crosslink Random Timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

**Notes:**

- 1.) No test load is necessarily associated with this value.
- 2.) Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 41](#) and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in [Figure 39](#))
- 3.) A  $T_{\text{TX-EYE}} = 0.70$  UI provides for a total sum of deterministic and random jitter budget of  $T_{\text{TX-JITTER-MAX}} = 0.30$  UI for the Transmitter collected over any 250 consecutive TX UIs. The  $T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$  median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4.) The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see [Figure 41](#)). Note that the series capacitors  $C_{\text{TX}}$  is optional for the return loss measurement.
- 5.) Measured between 20-80% at transmitter package pins into a test load as shown in [Figure 41](#) for both  $V_{\text{TX-D+}}$  and  $V_{\text{TX-D-}}$ .
- 6.) See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
- 7.) See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a

## 16.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in [Figure 39](#) is specified using the passive compliance/test measurement load (see [Figure 41](#)) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

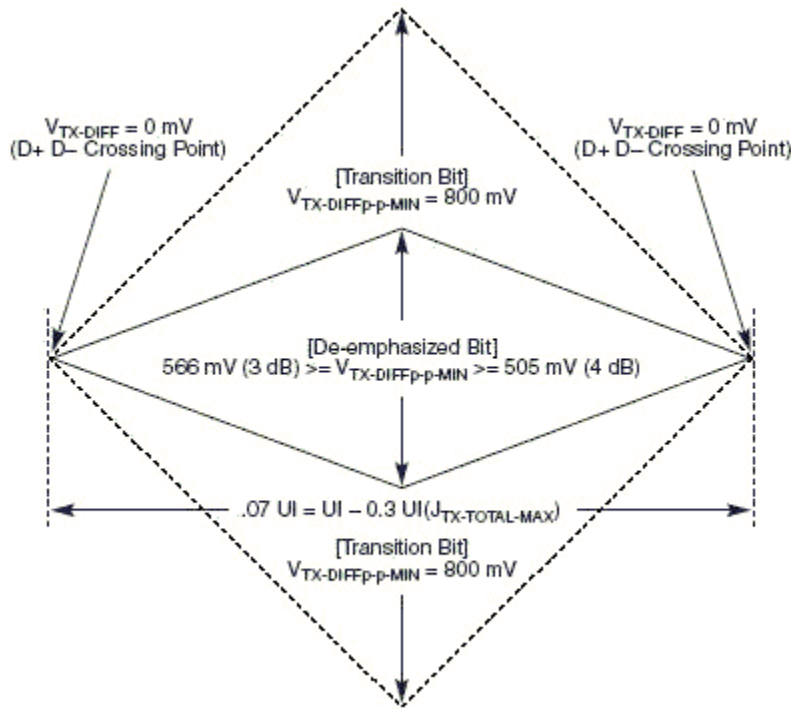


Figure 39. Minimum Transmitter Timing and Voltage Output Compliance Specifications

### 16.4.3 Differential Receiver (RX) Input Specifications

Table 53 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 53. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Input Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2 *  V_{RX-D+} - V_{RX-D-} $ See Note 2.
$T_{RX-EYE}$	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6 UI$ . See Notes 2 and 3.

Table 53. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-ACp} =  V_{RXD+} - V_{RXD-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $ V_{RX-D+} - V_{RX-D-} /2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
$RL_{RX-CM}$	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	$\Omega$	RX DC Differential mode impedance. See Note 5
$Z_{RX-DC}$	DC Input Impedance	40	50	60	$\Omega$	Required RX D+ as well as D- DC Impedance ( $50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			$\Omega$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 *  V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ( $V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$ ) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

**Table 53. Differential Receiver (RX) Input Specifications (continued)**

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1.) No test load is necessarily associated with this value.
- 2.) Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 41](#) should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in [Figure 40](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3.) A  $T_{RX-EYE} = 0.40$  UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4.) The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see [Figure 41](#)). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5.) Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 6.) The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7.) It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 40](#) is specified using the passive compliance/test measurement load (see [Figure 41](#)) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 41](#)) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in [Figure 40](#)) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

#### NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 41). Note that the series capacitors, C<sub>TX</sub>, are optional for the return loss measurement.

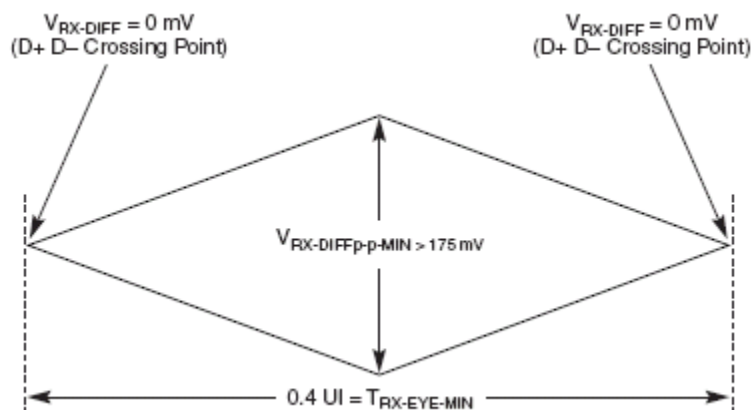


Figure 40. Minimum Receiver Eye Timing and Voltage Compliance Specification

### 16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 41.

#### NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.

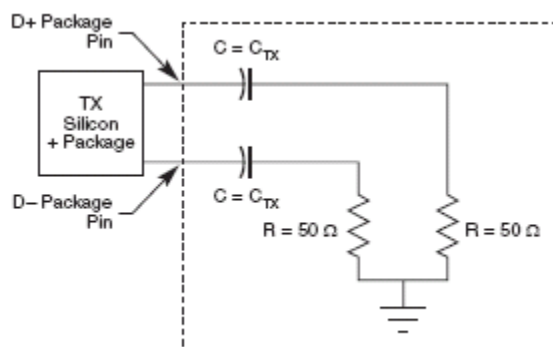


Figure 41. Compliance Test/Measurement Load

## 17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8548E, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of  $\pm 100$  ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

### 17.1 DC Requirements for Serial RapidIO SD\_REF\_CLK and SD\_REF\_CLK

For more information, see [Section 15.1, “DC Requirements for SerDes Reference Clocks.”](#)

### 17.2 AC Requirements for Serial RapidIO SD\_REF\_CLK and SD\_REF\_CLK

[Table 54](#) lists AC requirements.

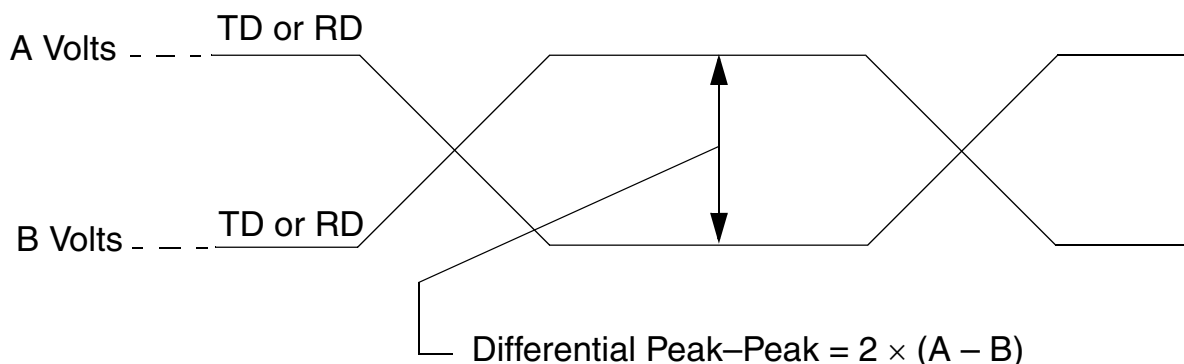
**Table 54. SD<sub>n</sub>\_REF\_CLK and  $\overline{\text{SD}}_n\text{\_REF\_CLK}$  AC Requirements**

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
$t_{\text{REF}}$	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
$t_{\text{REFCJ}}$	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
$t_{\text{REFPJ}}$	Phase jitter. Deviation in edge location with respect to mean edge location	-40	—	40	ps	

## 17.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 42 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and  $\overline{\text{TD}}$ ) or a receiver input (RD and  $\overline{\text{RD}}$ ). Each signal swings between A Volts and B Volts where  $A > B$ . Using these waveforms, the definitions are as follows:

3. The transmitter output signals and the receiver input signals TD,  $\overline{\text{TD}}$ , RD and  $\overline{\text{RD}}$  each have a peak-to-peak swing of  $A - B$  Volts
4. The differential output signal of the transmitter,  $V_{\text{OD}}$ , is defined as  $V_{\text{TD}} - V_{\overline{\text{TD}}}$
5. The differential input signal of the receiver,  $V_{\text{ID}}$ , is defined as  $V_{\text{RD}} - V_{\overline{\text{RD}}}$
6. The differential output signal of the transmitter and the differential input signal of the receiver each range from  $A - B$  to  $-(A - B)$  Volts
7. The peak value of the differential transmitter output signal and the differential receiver input signal is  $A - B$  Volts
8. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is  $2 * (A - B)$  Volts



**Figure 42. Differential Peak-Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and  $\overline{\text{TD}}$ , has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and  $\overline{\text{TD}}$  is 500 mV p-p. The differential output signal ranges between 500 mV and  $-500$  mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

## 17.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 17.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 17.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss,  $S_{11}$ , of the transmitter in each case shall be better than

- $-10$  dB for  $(\text{Baud Frequency})/10 < \text{Freq}(f) < 625$  MHz, and
- $-10$  dB +  $10\log(f/625 \text{ MHz})$  dB for  $625 \text{ MHz} \leq \text{Freq}(f) \leq \text{Baud Frequency}$

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

**Table 55. Short Run Transmitter AC Timing Specifications—1.25 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	500	1000	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	
Multiple output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

**Table 56. Short Run Transmitter AC Timing Specifications—2.5 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	500	1000	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	
Multiple Output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

**Table 57. Short Run Transmitter AC Timing Specifications—3.125 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	500	1000	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	

Table 57. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

Table 58. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	800	1600	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	
Multiple output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 59. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	800	1600	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	
Multiple output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 60. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	$V_O$	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	800	1600	mV p-p	
Deterministic Jitter	$J_D$		0.17	UI p-p	
Total Jitter	$J_T$		0.35	UI p-p	
Multiple output skew	$S_{MO}$		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 43 with the parameters specified in Table 61 when measured at the output pins of the device and the device is driving a 100 Ohm +/-5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

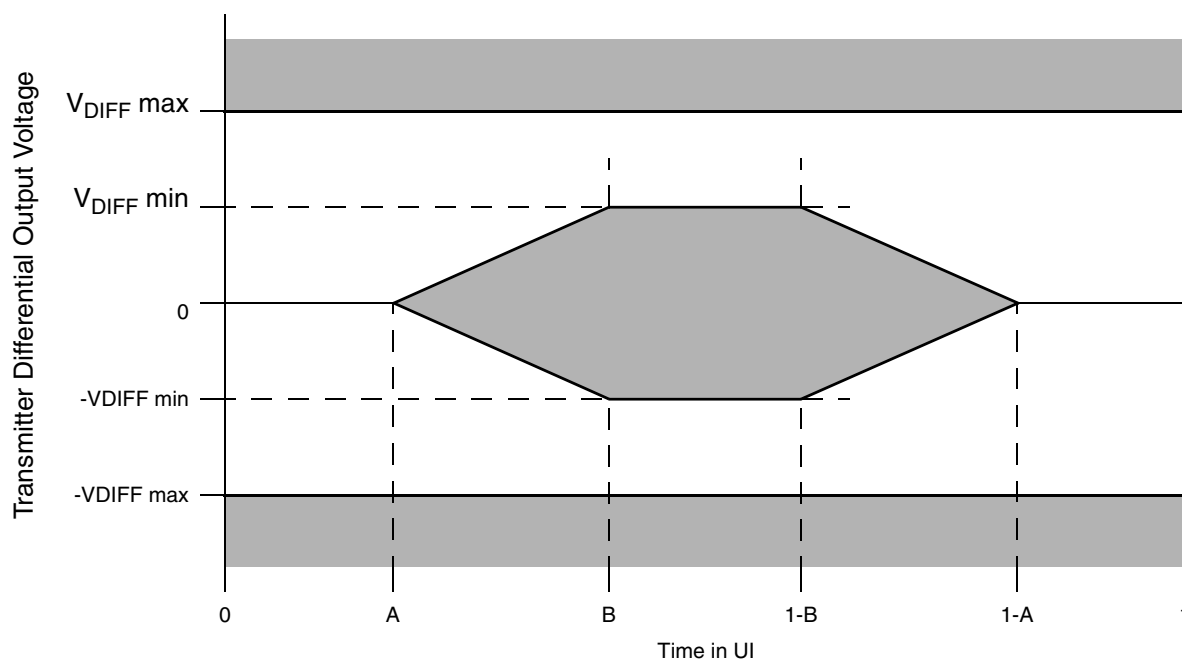


Figure 43. Transmitter Output Compliance Mask

**Table 61. Transmitter Differential Output Eye Diagram Parameters**

Transmitter Type	V <sub>DIFFmin</sub> (mV)	V <sub>DIFFmax</sub> (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

## 17.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to  $(0.8) \times (\text{Baud Frequency})$ . This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

**Table 62. Receiver AC Timing Specifications—1.25 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V <sub>IN</sub>	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J <sub>D</sub>	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J <sub>DR</sub>	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance <sup>1</sup>	J <sub>T</sub>	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S <sub>MI</sub>		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10 <sup>-12</sup>		
Unit Interval	UI	800	800	ps	+/- 100 ppm

**Note:**

- Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 44](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Table 63. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	$J_D$	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	$J_{DR}$	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance <sup>1</sup>	$J_T$	0.65		UI p-p	Measured at receiver
Multiple Input Skew	$S_{MI}$		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		$10^{-12}$		
Unit Interval	UI	400	400	ps	+/- 100 ppm

**Note:**

- Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 44](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 64. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	$J_D$	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	$J_{DR}$	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance <sup>1</sup>	$J_T$	0.65		UI p-p	Measured at receiver
Multiple Input Skew	$S_{MI}$		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		$10^{-12}$		
Unit Interval	UI	320	320	ps	+/- 100 ppm

**Note:**

- Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 44](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

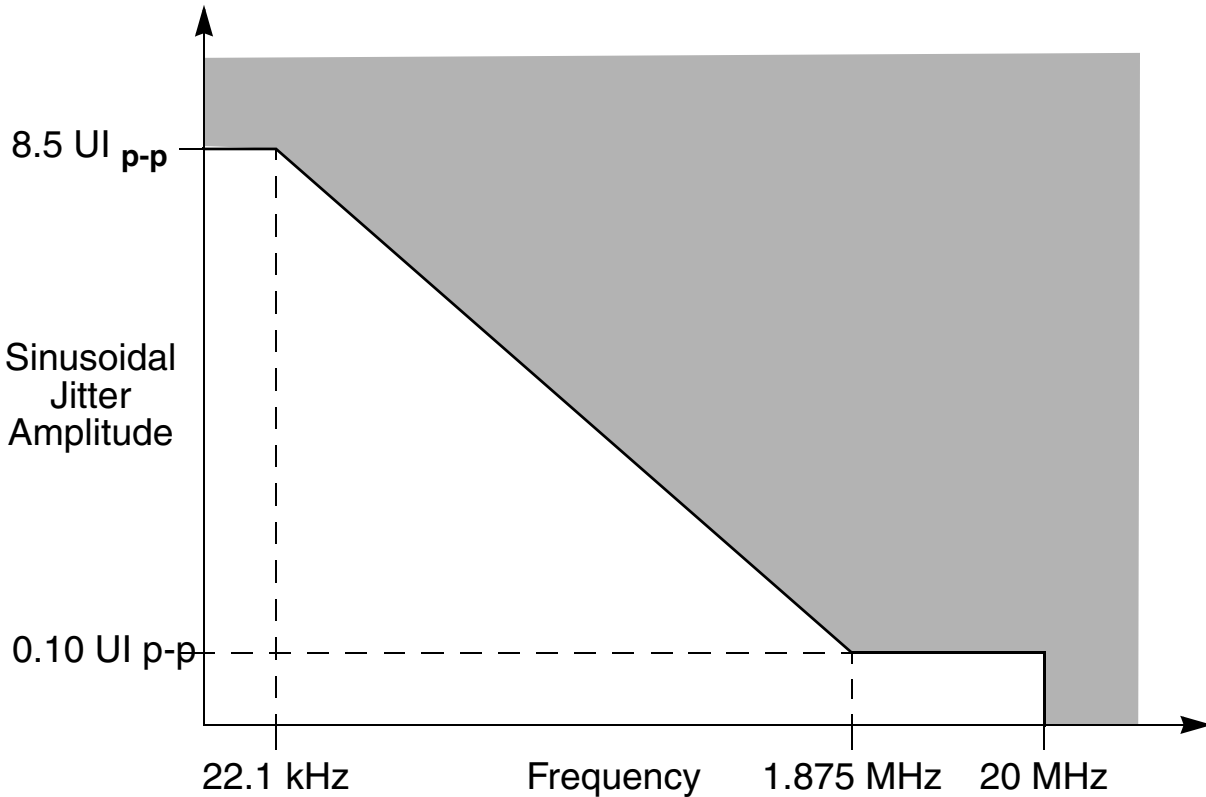


Figure 44. Single Frequency Sinusoidal Jitter Limits

## 17.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 62, Table 63, Table 64) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 45 with the parameters specified in Table 65. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ohm  $\pm$  5% differential resistive load.

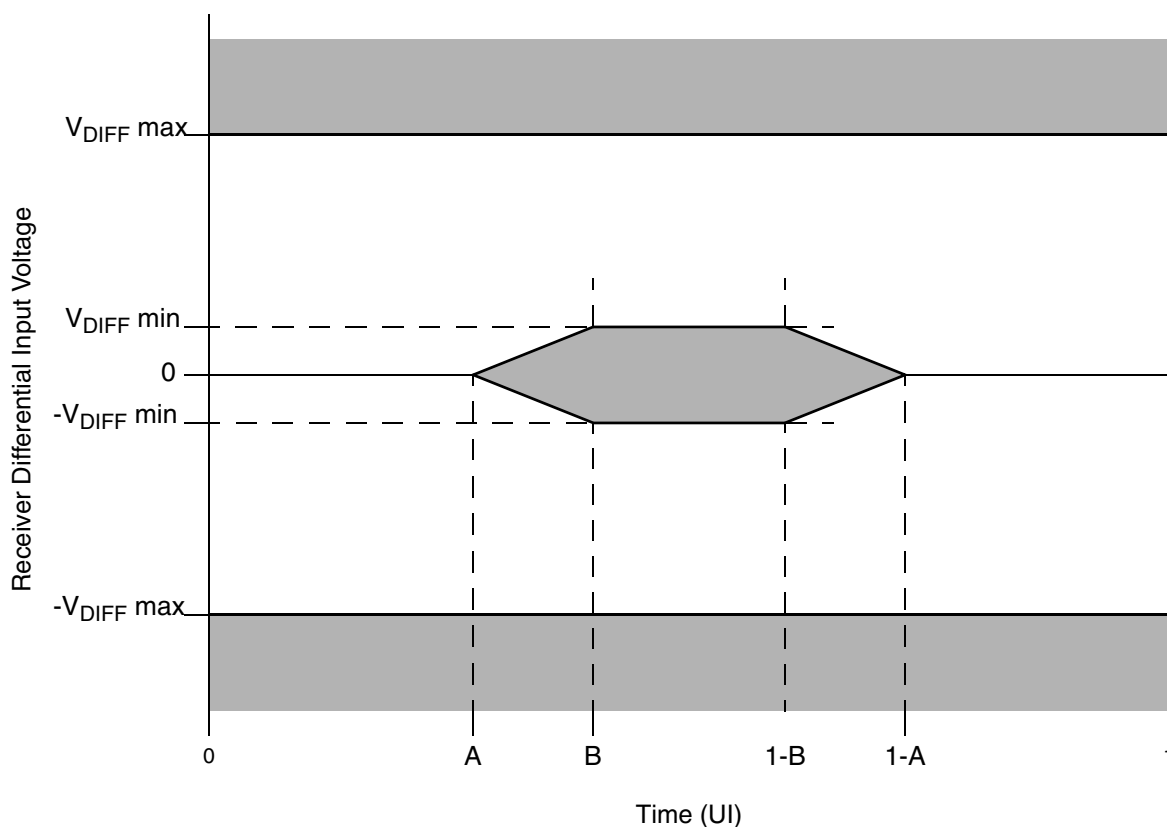


Figure 45. Receiver Input Compliance Mask

Table 65. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	$V_{DIFF\ min}$ (mV)	$V_{DIFF\ max}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

## 17.9 Measurement and Test Requirements

Since the LP-Serial electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

## 17.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than  $10^{-12}$ . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive +/- 5% differential to 2.5 GHz.

## 17.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE Std. 802.3ae.

## 17.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive +/- 5% differential to 2.5 GHz.

## 17.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

## 18 Package Description

This section details package parameters, pin assignments, and dimensions.

### 18.1 Package Parameters

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are as provided in [Table 66](#).

**Table 66. Package Parameters**

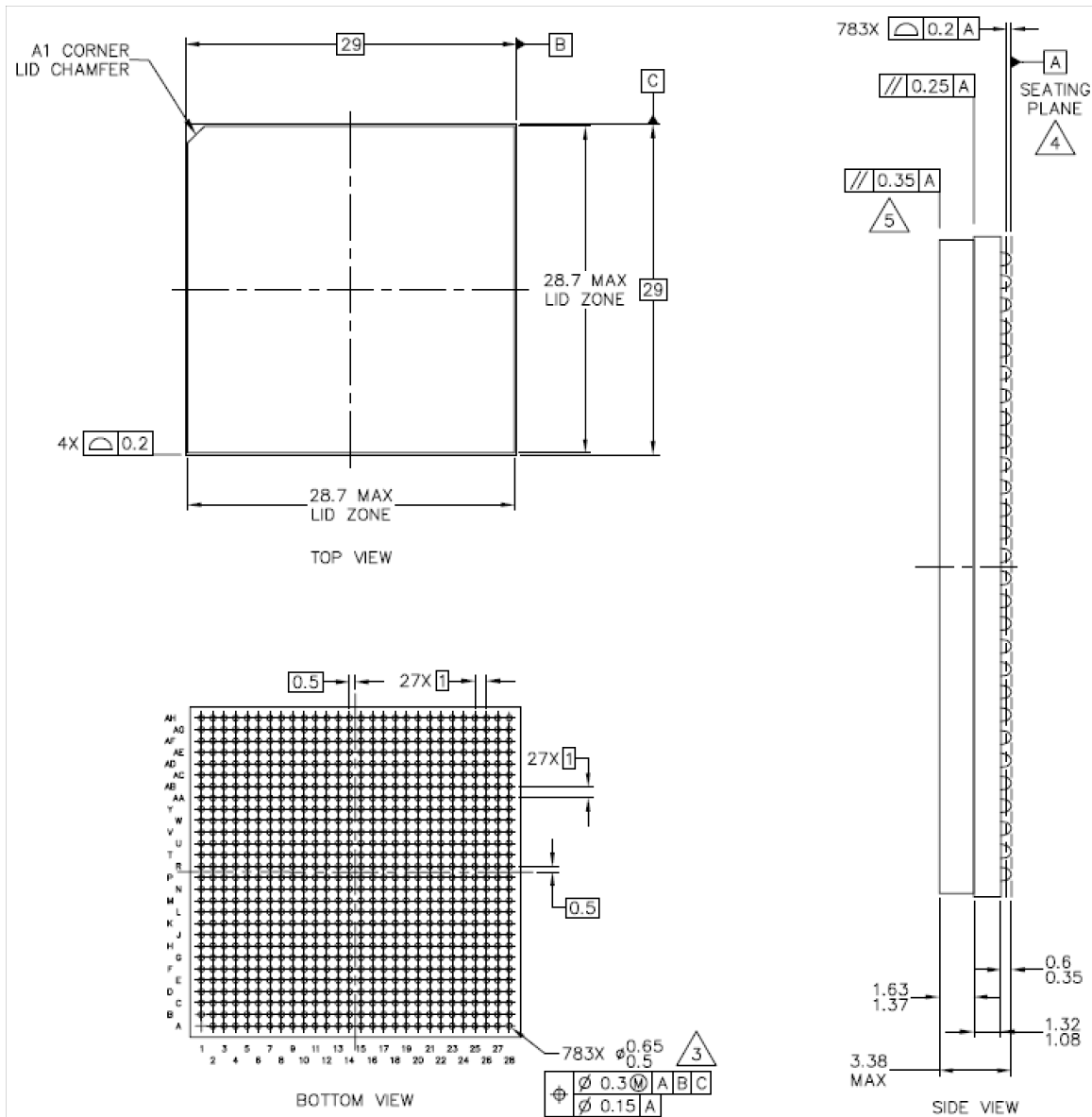
Parameter	CBGA <sup>1</sup>	PBGA <sup>2</sup>
Package Outline	29 mm x 29 mm	29 mm x 29 mm
Interconnects	783	783
Ball Pitch	1 mm	1 mm
Ball Diameter (Typical)	0.6 mm	0.6 mm
Solder Ball	62% Sn 36% Pb 2% Ag	62% Sn 36% Pb 2% Ag
Solder Ball (Lead-Free)	95% Sn 4.5% Ag 0.5% Cu	96.5% Sn 3.5% Ag

**Note:**

1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
2. The FC-PBGA package is available on only Version 2.1 of the device.

### 18.2 Mechanical Dimensions of the HiCTE FC-CBGA and FC-PBGA with Full Lid

[Figure 46](#) shows the mechanical dimensions and bottom surface nomenclature for both the MPC8548E HiCTE FC-CBGA and FC-PBGA package with full lid.



**Figure 46. Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid**

**NOTES**

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
7. Package code summary:
 

• PBGA	8423
• CBGA	5112

## 18.3 Pinout Listings

### NOTE

The  $\overline{\text{DMA\_DACK}}[0:1]$  and  $\overline{\text{TEST\_SEL}}/\overline{\text{TEST\_SEL}}$  pins must be set to a proper state during POR configuration. Please refer to the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on  $\text{PCI1\_AD}[63:32]/\text{PC2\_AD}[31:0]$  pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 67 provides the pin-out listing for the MPC8548E 783 FC-PBGA package.

**Table 67. MPC8548E Pinout Listing**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 and PCI2 (one 64-bit or two 32-bit)</b>				
$\text{PCI1\_AD}[63:32]/\text{PCI2\_AD}[31:0]$	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	$\text{OV}_{\text{DD}}$	17
$\text{PCI1\_AD}[31:0]$	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	$\text{OV}_{\text{DD}}$	17
$\text{PCI1\_C\_}\overline{\text{BE}}[7:4]/\text{PCI2\_C\_}\overline{\text{BE}}[3:0]$	AF15, AD14, AE15, AD15	I/O	$\text{OV}_{\text{DD}}$	17
$\text{PCI1\_C\_}\overline{\text{BE}}[3:0]$	AF9, AD11, Y12, Y13	I/O	$\text{OV}_{\text{DD}}$	17
$\text{PCI1\_PAR}64/\text{PCI2\_PAR}$	W15	I/O	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_GNT}}[4:1]$	AG6, AE6, AF5, AH5	O	$\text{OV}_{\text{DD}}$	5,9,35
$\overline{\text{PCI1\_GNT}}0$	AG5	I/O	$\text{OV}_{\text{DD}}$	
$\text{PCI1\_IRDY}$	AF11	I/O	$\text{OV}_{\text{DD}}$	2
$\text{PCI1\_PAR}$	AD12	I/O	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	$\text{OV}_{\text{DD}}$	2,4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	$\text{OV}_{\text{DD}}$	2
$\text{PCI1\_TRDY}$	AG11	I/O	$\text{OV}_{\text{DD}}$	2
$\text{PCI1\_REQ}[4:1]$	AH2, AG4, AG3, AH4	I	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_REQ}}0$	AH3	I/O	$\text{OV}_{\text{DD}}$	
$\text{PCI1\_CLK}$	AH26	I	$\text{OV}_{\text{DD}}$	39
$\overline{\text{PCI1\_DEVSEL}}$	AH11	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_FRAME}}$	AE11	I/O	$\text{OV}_{\text{DD}}$	2

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_IDSEL	AG9	I	OV <sub>DD</sub>	
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV <sub>DD</sub>	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV <sub>DD</sub>	2
PCI2_CLK	AE28	I	OV <sub>DD</sub>	39
PCI2_IRDY	AD26	I/O	OV <sub>DD</sub>	2
PCI2_PERR	AD25	I/O	OV <sub>DD</sub>	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	O	OV <sub>DD</sub>	5,9,35
PCI2_GNT0	AG25	I/O	OV <sub>DD</sub>	
PCI2_SERR	AD24	I/O	OV <sub>DD</sub>	2,4
PCI2_STOP	AF24	I/O	OV <sub>DD</sub>	2
PCI2_TRDY	AD27	I/O	OV <sub>DD</sub>	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV <sub>DD</sub>	
PCI2_REQ0	AH25	I/O	OV <sub>DD</sub>	
<b>DDR SDRAM Memory Interface</b>				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV <sub>DD</sub>	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV <sub>DD</sub>	
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV <sub>DD</sub>	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV <sub>DD</sub>	
MBA[0:2]	F7, J7, M11	O	GV <sub>DD</sub>	
MWE	E7	O	GV <sub>DD</sub>	
MCAS	H7	O	GV <sub>DD</sub>	
MRAS	L8	O	GV <sub>DD</sub>	
MCKE[0:3]	F10, C10, J11, H11	O	GV <sub>DD</sub>	11
MCS[0:3]	K8, J8, G8, F8	O	GV <sub>DD</sub>	
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV <sub>DD</sub>	
MCK[0:5]	J9, A15, G1, L9, B14, F2	O	GV <sub>DD</sub>	
MODT[0:3]	E6, K6, L7, M7	O	GV <sub>DD</sub>	
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36



Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Local Bus Controller Interface</b>				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	
LA[27]	H21	O	BV <sub>DD</sub>	5,9
LA[28:31]	H20, A27, D26, A28	O	BV <sub>DD</sub>	5,7,9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV <sub>DD</sub>	
$\overline{\text{LCS5/DMA\_DREQ2}}$	D23	I/O	BV <sub>DD</sub>	1
$\overline{\text{LCS6/DMA\_DACK2}}$	G20	O	BV <sub>DD</sub>	1
$\overline{\text{LCS7/DMA\_DDONE2}}$	E21	O	BV <sub>DD</sub>	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV <sub>DD</sub>	5,9
LALE	H24	O	BV <sub>DD</sub>	5,8,9
LBCTL	G27	O	BV <sub>DD</sub>	5,8,9
LGPL0/LSDA10	F23	O	BV <sub>DD</sub>	5,9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV <sub>DD</sub>	5,9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV <sub>DD</sub>	5,8,9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV <sub>DD</sub>	5,9
LGPL4/ $\overline{\text{LGTA/LUPWAIT/LPBSE}}$	H23	I/O	BV <sub>DD</sub>	
LGPL5	E26	O	BV <sub>DD</sub>	5,9
LCKE	E24	O	BV <sub>DD</sub>	
LCLK[0:2]	E23, D24, H22	O	BV <sub>DD</sub>	
LSYNC_IN	F27	I	BV <sub>DD</sub>	
LSYNC_OUT	F28	O	BV <sub>DD</sub>	
<b>DMA</b>				
DMA_DACK[0:1]	AD3, AE1	O	OV <sub>DD</sub>	5,9,102
$\overline{\text{DMA\_DREQ}}[0:1]$	AD4, AE2	I	OV <sub>DD</sub>	
$\overline{\text{DMA\_DDONE}}[0:1]$	AD2, AD1	O	OV <sub>DD</sub>	
<b>Programmable Interrupt Controller</b>				
$\overline{\text{UDE}}$	AH16	I	OV <sub>DD</sub>	

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCP}}$	AG19	I	$\text{OV}_{\text{DD}}$	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	$\text{OV}_{\text{DD}}$	
IRQ[8]	AF19	I	$\text{OV}_{\text{DD}}$	
IRQ[9]/ $\overline{\text{DMA\_DREQ3}}$	AF21	I	$\text{OV}_{\text{DD}}$	1
IRQ[10]/ $\overline{\text{DMA\_DACK3}}$	AE19	I/O	$\text{OV}_{\text{DD}}$	1
IRQ[11]/ $\overline{\text{DMA\_DDONE3}}$	AD20	I/O	$\text{OV}_{\text{DD}}$	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	$\text{OV}_{\text{DD}}$	2,4
<b>Ethernet Management Interface</b>				
EC_MDC	AB9	O	$\text{OV}_{\text{DD}}$	5,9
EC_MDIO	AC8	I/O	$\text{OV}_{\text{DD}}$	
<b>Gigabit Reference Clock</b>				
EC_GTX_CLK125	V11	I	$\text{LV}_{\text{DD}}$	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b>				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	$\text{LV}_{\text{DD}}$	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	$\text{LV}_{\text{DD}}$	5, 9
TSEC1_COL	R4	I	$\text{LV}_{\text{DD}}$	
TSEC1_CRS	V5	I/O	$\text{LV}_{\text{DD}}$	20
TSEC1_GTX_CLK	U7	O	$\text{LV}_{\text{DD}}$	
TSEC1_RX_CLK	U3	I	$\text{LV}_{\text{DD}}$	
TSEC1_RX_DV	V2	I	$\text{LV}_{\text{DD}}$	
TSEC1_RX_ER	T1	I	$\text{LV}_{\text{DD}}$	
TSEC1_TX_CLK	T6	I	$\text{LV}_{\text{DD}}$	
TSEC1_TX_EN	U9	O	$\text{LV}_{\text{DD}}$	30
TSEC1_TX_ER	T7	O	$\text{LV}_{\text{DD}}$	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 2)</b>				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	$\text{LV}_{\text{DD}}$	
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	$\text{LV}_{\text{DD}}$	5, 9, 33
TSEC2_COL	P1	I	$\text{LV}_{\text{DD}}$	
TSEC2_CRS	R6	I/O	$\text{LV}_{\text{DD}}$	20
TSEC2_GTX_CLK	P6	O	$\text{LV}_{\text{DD}}$	
TSEC2_RX_CLK	N4	I	$\text{LV}_{\text{DD}}$	
TSEC2_RX_DV	P5	I	$\text{LV}_{\text{DD}}$	

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_RX_ER	R1	I	LV <sub>DD</sub>	
TSEC2_TX_CLK	P10	I	LV <sub>DD</sub>	
TSEC2_TX_EN	P7	O	LV <sub>DD</sub>	30
TSEC2_TX_ER	R10	O	LV <sub>DD</sub>	5, 9, 33
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 3)</b>				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	
TSEC3_GTX_CLK	W8	O	TV <sub>DD</sub>	
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	
TSEC3_TX_EN	V9	O	TV <sub>DD</sub>	30
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 4)</b>				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV <sub>DD</sub>	1,5,9,29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	1
TSEC4_GTX_CLK	AA5	O	TV <sub>DD</sub>	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV <sub>DD</sub>	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	1,31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV <sub>DD</sub>	1,30
<b>DUART</b>				
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	
UART_RTS[0:1]	AC6, AD7	O	OV <sub>DD</sub>	
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	
UART_SOUT[0:1]	AB7, AD8	O	OV <sub>DD</sub>	
<b>I<sup>2</sup>C interface</b>				
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4,27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4,27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4,27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4,27
<b>SerDes</b>				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV <sub>DD</sub>	
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV <sub>DD</sub>	

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV <sub>DD</sub>	
$\overline{\text{SD\_TX}}$ [0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV <sub>DD</sub>	
SD_PLL_TPD	U28	O	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV <sub>DD</sub>	
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
<b>General-Purpose Output</b>				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV <sub>DD</sub>	
<b>System Control</b>				
$\overline{\text{HRESET}}$	AG17	I	OV <sub>DD</sub>	
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV <sub>DD</sub>	29
$\overline{\text{SRESET}}$	AG20	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV <sub>DD</sub>	2,4
<b>Debug</b>				
TRIG_IN	AB2	I	OV <sub>DD</sub>	
$\overline{\text{TRIG\_OUT/READY/QUIESCE}}$	AB1	O	OV <sub>DD</sub>	6,9,19,29
MSRCID[0:1]	AE4, AG2	O	OV <sub>DD</sub>	5,6,9
MSRCID[2:4]	AF3, AF1, AF2	O	OV <sub>DD</sub>	6,19,29
MDVAL	AE5	O	OV <sub>DD</sub>	6
CLK_OUT	AE21	O	OV <sub>DD</sub>	11
<b>Clock</b>				
RTC	AF16	I	OV <sub>DD</sub>	
SYSCLK	AH17	I	OV <sub>DD</sub>	
<b>JTAG</b>				
TCK	AG28	I	OV <sub>DD</sub>	
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	O	OV <sub>DD</sub>	11
TMS	AH27	I	OV <sub>DD</sub>	12

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{TRST}}$	AH23	I	OV <sub>DD</sub>	12
<b>DFT</b>				
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV <sub>DD</sub>	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV <sub>DD</sub>	25
<b>Thermal Management</b>				
THERM0	AG1		—	14
THERM1	AH1		—	14
<b>Power Management</b>				
ASLEEP	AH18	O	OV <sub>DD</sub>	9,19,29
<b>Power and Ground Signals</b>				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27 K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28 L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21 U27	—	—	
OVDD	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3V)	OVDD	
LVDD	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5V, 3.3V)	LVDD	
TVDD	W9, Y6	Power for TSEC3 and TSEC4 (2.5V, 3.3V)	TVDD	

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V,2.5V)	GVDD	
BVDD	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	
VDD	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for Core (1.1 V)	VDD	
SVDD	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SVDD	
XVDD	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XVDD	
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)		26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)		26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)		26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	O	V <sub>DD</sub>	13
SENSEVSS	M16			13

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Analog Signals</b>				
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	O		24

Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
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**Notes:**

1. All multiplexed signals are listed only once and do not re-occur. For example,  $\overline{\text{LCS5/DMA\_REQ2}}$  is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as  $\overline{\text{DMA\_REQ2}}$ .
2. Recommend a weak pull-up resistor (2–10 K $\Omega$ ) be placed on this pin to  $\text{OV}_{\text{DD}}$ .
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k $\Omega$  pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSClk PLL ratio. These pins require 4.7-k $\Omega$  pull-up or pull-down resistors. See Section 19.2, “CCB/SYSClk PLL Ratio.”
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k $\Omega$  pull-up or pull-down resistors. See the Section 19.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the  $\text{V}_{\text{DD}}/\text{GND}$  planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins if they are not used.
16. These pins are not connected for any use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 K $\Omega$ ) be placed on the higher order pins to  $\text{OV}_{\text{DD}}$  when using 64-bit buffer mode (pins PCI\_AD[63:32] and  $\overline{\text{PCI1\_C\_BE}}$ [7:4]).
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx Flow Control.
24. Do not connect.
25. These are test signals for factory use only and must be pulled up (100 . - 1 k.) to  $\text{OV}_{\text{DD}}$  for normal machine operation.
26. Independent supplies derived from board VDD.
27. Recommend a pull-up resistor (~1 k $\Omega$ .) be placed on this pin to  $\text{OV}_{\text{DD}}$ .
29. The following pins must NOT be pulled down during power-on reset: TSEC3\_TXD[3], TSEC4\_TXD3/TSEC3\_TXD7, HRESET\_REQ, TRIG\_OUT/READY/ $\overline{\text{QUIESCE}}$ , MSRCID[2:4], ASLEEP.  
For rev 2.0 silicon,



Table 67. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
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30. This pin requires an external 4.7-k $\Omega$  pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
31. This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.
32. These pins should be connected to  $XV_{DD}$ .
33. TSEC2\_TXD1, TSEC2\_TX\_ER are multiplexed as `cfg_dram_type[0:1]`. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE  $\overline{HRESET}$  ASSERTION.
34. These pins should be pulled to ground through a 300- $\Omega$  ( $\pm 10\%$ ) resistor.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the  $PCI_n\_AD$  pins as "No Connect" or terminated through 2–10 K $\Omega$  pull-up resistors with the default of internal arbiter if the  $PCI_n\_AD$  pins are not connected to any other PCI device. The PCI block will drive the  $PCI_n\_AD$  pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC0 is grounded through an 18.2- $\Omega$  precision 1% resistor and MDIC1 is connected to  $GV_{DD}$  through an 18.2- $\Omega$  precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
38. These pins should be left floating.
39. If PCI1 or PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1\_CLK or PCI2\_CLK. Otherwise the processor will not boot up.
40. These pins should be connected to GND.
101. This pin requires an external 4.7-K $\Omega$  resistor to GND.
102. For Rev. 2.0 silicon,  $\overline{DMA\_DACK}[0:1]$  must be 0b11 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
103. If these pins are not used as GPINn (general-purpose input), they should be pulled low (to GND) or high (to  $LV_{DD}$ ) through 2–10 K $\Omega$  resistors.
104. These should be pulled low to GND through 2–10 K $\Omega$  resistors if they are not used.
105. These should be pulled low or high to  $LV_{DD}$  through 2–10 K $\Omega$  resistors if they are not used.
106. For Rev. 2.0 silicon,  $\overline{DMA\_DACK}[0:1]$  must be 0b10 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
107. For Rev. 2.0 silicon,  $\overline{DMA\_DACK}[0:1]$  must be 0b01 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
108. For Rev. 2.0 silicon,  $\overline{DMA\_DACK}[0:1]$  must be 0b11 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
109. This is a test signal for factory use only and must be pulled down (100  $\Omega$  – 1 K $\Omega$ ) to GND for normal machine operation.
110. These pins should be pulled high to  $OV_{DD}$  through 2–10 K $\Omega$  resistors.
111. If these pins are not used as GPINn (general-purpose input), they should be pulled low (to GND) or high (to  $OV_{DD}$ ) through 2–10 K $\Omega$  resistors.
112. This pin must not be pulled down during POR configuration.
113. These should be pulled low or high to  $OV_{DD}$  through 2–10 K $\Omega$  resistors.

Table 68 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

**NOTE**

All note references in the following table use the same numbers as those for Table 67. The reader should refer to Table 67 for the meanings of these notes.

**Table 68. MPC8547E Pinout Listing**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 (one 64-bit or one 32-bit)</b>				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV <sub>DD</sub>	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
PCI1_C $\overline{\text{BE}}$ [7:4]	AF15, AD14, AE15, AD15	I/O	OV <sub>DD</sub>	17
PCI1_C $\overline{\text{BE}}$ [3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
PCI1_PAR64	W15	I/O	OV <sub>DD</sub>	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5,9,35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2,4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2
PCI1_TRDY	AG11	I/O	OV <sub>DD</sub>	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV <sub>DD</sub>	
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2
PCI1_FRAME	AE11	I/O	OV <sub>DD</sub>	2
PCI1_IDSEL	AG9	I	OV <sub>DD</sub>	
PCI1_REQ64	AF14	I/O	OV <sub>DD</sub>	2, 5,10
PCI1_ACK64	V15	I/O	OV <sub>DD</sub>	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV <sub>DD</sub>	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
<b>DDR SDRAM Memory Interface</b>				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV <sub>DD</sub>	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV <sub>DD</sub>	
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV <sub>DD</sub>	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	
$\overline{\text{MDQS}}$ [0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV <sub>DD</sub>	
MBA[0:2]	F7, J7, M11	O	GV <sub>DD</sub>	
$\overline{\text{MWE}}$	E7	O	GV <sub>DD</sub>	
$\overline{\text{MCAS}}$	H7	O	GV <sub>DD</sub>	
$\overline{\text{MRAS}}$	L8	O	GV <sub>DD</sub>	
MCKE[0:3]	F10, C10, J11, H11	O	GV <sub>DD</sub>	11
$\overline{\text{MCS}}$ [0:3]	K8, J8, G8, F8	O	GV <sub>DD</sub>	
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV <sub>DD</sub>	
$\overline{\text{MCK}}$ [0:5]	J9, A15, G1, L9, B14, F2	O	GV <sub>DD</sub>	
MODT[0:3]	E6, K6, L7, M7	O	GV <sub>DD</sub>	
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36
<b>Local Bus Controller Interface</b>				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	

Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	
LA[27]	H21	O	BV <sub>DD</sub>	5,9
LA[28:31]	H20, A27, D26, A28	O	BV <sub>DD</sub>	5,7,9
$\overline{\text{LCS}}$ [0:4]	J25, C20, J24, G26, A26	O	BV <sub>DD</sub>	
$\overline{\text{LCS5/DMA\_DREQ2}}$	D23	I/O	BV <sub>DD</sub>	1
$\overline{\text{LCS6/DMA\_DACK2}}$	G20	O	BV <sub>DD</sub>	1
$\overline{\text{LCS7/DMA\_DDONE2}}$	E21	O	BV <sub>DD</sub>	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV <sub>DD</sub>	5,9
LALE	H24	O	BV <sub>DD</sub>	5,8,9
LBCTL	G27	O	BV <sub>DD</sub>	5,8,9
LGPL0/LSDA10	F23	O	BV <sub>DD</sub>	5,9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV <sub>DD</sub>	5,9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV <sub>DD</sub>	5,8,9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV <sub>DD</sub>	5,9
LGPL4/ $\overline{\text{LGT\AA/LUPWAIT/LPBSE}}$	H23	I/O	BV <sub>DD</sub>	
LGPL5	E26	O	BV <sub>DD</sub>	5,9
LCKE	E24	O	BV <sub>DD</sub>	
LCLK[0:2]	E23, D24, H22	O	BV <sub>DD</sub>	
LSYNC_IN	F27	I	BV <sub>DD</sub>	
LSYNC_OUT	F28	O	BV <sub>DD</sub>	
<b>DMA</b>				
$\overline{\text{DMA\_DACK}}[0:1]$	AD3, AE1	O	OV <sub>DD</sub>	5,9,107
$\overline{\text{DMA\_DREQ}}[0:1]$	AD4, AE2	I	OV <sub>DD</sub>	
$\overline{\text{DMA\_DDONE}}[0:1]$	AD2, AD1	O	OV <sub>DD</sub>	
<b>Programmable Interrupt Controller</b>				
$\overline{\text{UDE}}$	AH16	I	OV <sub>DD</sub>	
$\overline{\text{MCP}}$	AG19	I	OV <sub>DD</sub>	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV <sub>DD</sub>	
IRQ[8]	AF19	I	OV <sub>DD</sub>	
IRQ[9]/ $\overline{\text{DMA\_DREQ3}}$	AF21	I	OV <sub>DD</sub>	1
IRQ[10]/ $\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV <sub>DD</sub>	1

Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[11]/DMA_DDONE3	AD20	I/O	OV <sub>DD</sub>	1
IRQ_OUT	AD18	O	OV <sub>DD</sub>	2,4
<b>Ethernet Management Interface</b>				
EC_MDC	AB9	O	OV <sub>DD</sub>	5,9
EC_MDIO	AC8	I/O	OV <sub>DD</sub>	
<b>Gigabit Reference Clock</b>				
EC_GTX_CLK125	V11	I	LV <sub>DD</sub>	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b>				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV <sub>DD</sub>	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV <sub>DD</sub>	5, 9
TSEC1_COL	R4	I	LV <sub>DD</sub>	
TSEC1_CRS	V5	I/O	LV <sub>DD</sub>	20
TSEC1_GTX_CLK	U7	O	LV <sub>DD</sub>	
TSEC1_RX_CLK	U3	I	LV <sub>DD</sub>	
TSEC1_RX_DV	V2	I	LV <sub>DD</sub>	
TSEC1_RX_ER	T1	I	LV <sub>DD</sub>	
TSEC1_TX_CLK	T6	I	LV <sub>DD</sub>	
TSEC1_TX_EN	U9	O	LV <sub>DD</sub>	30
TSEC1_TX_ER	T7	O	LV <sub>DD</sub>	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 2)</b>				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV <sub>DD</sub>	
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV <sub>DD</sub>	5, 9, 33
TSEC2_COL	P1	I	LV <sub>DD</sub>	
TSEC2_CRS	R6	I/O	LV <sub>DD</sub>	20
TSEC2_GTX_CLK	P6	O	LV <sub>DD</sub>	
TSEC2_RX_CLK	N4	I	LV <sub>DD</sub>	
TSEC2_RX_DV	P5	I	LV <sub>DD</sub>	
TSEC2_RX_ER	R1	I	LV <sub>DD</sub>	
TSEC2_TX_CLK	P10	I	LV <sub>DD</sub>	
TSEC2_TX_EN	P7	O	LV <sub>DD</sub>	30
TSEC2_TX_ER	R10	O	LV <sub>DD</sub>	5, 9, 33
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 3)</b>				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	

Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_GTX_CLK	W8	O	TV <sub>DD</sub>	
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	
TSEC3_TX_EN	V9	O	TV <sub>DD</sub>	30
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 4)</b>				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV <sub>DD</sub>	1,5,9,29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	1
TSEC4_GTX_CLK	AA5	O	TV <sub>DD</sub>	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV <sub>DD</sub>	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	1,31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV <sub>DD</sub>	1,30
<b>DUART</b>				
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	
UART_RTS[0:1]	AC6, AD7	O	OV <sub>DD</sub>	
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	
UART_SOUT[0:1]	AB7, AD8	O	OV <sub>DD</sub>	
<b>I<sup>2</sup>C interface</b>				
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4,27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4,27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4,27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4,27
<b>SerDes</b>				
SD_RX[0:3]	M28, N26, P28, R26	I	XV <sub>DD</sub>	
$\overline{\text{SD\_RX}}$ [0:3]	M27, N25, P27, R25	I	XV <sub>DD</sub>	
SD_TX[0:3]	M22, N20, P22, R20	O	XV <sub>DD</sub>	
$\overline{\text{SD\_TX}}$ [0:3]	M23, N21, P23, R21	O	XV <sub>DD</sub>	
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	

Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_REF_CLK	T27	I	XV <sub>DD</sub>	
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
<b>General-Purpose Output</b>				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV <sub>DD</sub>	
<b>System Control</b>				
$\overline{\text{HRESET}}$	AG17	I	OV <sub>DD</sub>	
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV <sub>DD</sub>	29
$\overline{\text{SRESET}}$	AG20	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV <sub>DD</sub>	2,4
<b>Debug</b>				
TRIG_IN	AB2	I	OV <sub>DD</sub>	
TRIG_OUT/READY/QUIESCE	AB1	O	OV <sub>DD</sub>	6,9,19,29
MSRCID[0:1]	AE4, AG2	O	OV <sub>DD</sub>	5,6,9
MSRCID[2:4]	AF3, AF1, AF2	O	OV <sub>DD</sub>	6,19,29
MDVAL	AE5	O	OV <sub>DD</sub>	6
CLK_OUT	AE21	O	OV <sub>DD</sub>	11
<b>Clock</b>				
RTC	AF16	I	OV <sub>DD</sub>	
SYSCLK	AH17	I	OV <sub>DD</sub>	
<b>JTAG</b>				
TCK	AG28	I	OV <sub>DD</sub>	
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	O	OV <sub>DD</sub>	11
TMS	AH27	I	OV <sub>DD</sub>	12
$\overline{\text{TRST}}$	AH23	I	OV <sub>DD</sub>	12
<b>DFT</b>				
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV <sub>DD</sub>	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV <sub>DD</sub>	25

**Table 68. MPC8547E Pinout Listing (continued)**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Thermal Management</b>				
THERM0	AG1		—	14
THERM1	AH1		—	14
<b>Power Management</b>				
ASLEEP	AH18	O	OV <sub>DD</sub>	9,19,29
<b>Power and Ground Signals</b>				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27 K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28 L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21 U27	—	—	
OVDD	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3V)	OVDD	
LVDD	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5V, 3.3V)	LVDD	
TVDD	W9, Y6	Power for TSEC3 and TSEC4 (2.5V, 3.3V)	TVDD	
GVDD	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V, 2.5V)	GVDD	
BVDD	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	
VDD	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for Core (1.1 V)	VDD	



Table 68. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SVDD	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SVDD	
XVDD	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XVDD	
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)		26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)		26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)		26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	O	V <sub>DD</sub>	13
SENSEVSS	M16			13
<b>Analog Signals</b>				
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	O		24

**Notes:**

All note references in this table use the same numbers as those for [Table 67](#). The reader should refer to [Table 67](#) for the meanings of these notes.

Table 69 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

**NOTE**

All note references in the following table use the same numbers as those for Table 67. The reader should refer to Table 67 for the meanings of these notes.

**Table 69. MPC8545E Pinout Listing**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 and PCI2 (one 64-bit or two 32-bit)</b>				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV <sub>DD</sub>	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
PCI1_C_B $\bar{E}$ [7:4]/PCI2_C_B $\bar{E}$ [3:0]	AF15, AD14, AE15, AD15	I/O	OV <sub>DD</sub>	17
PCI1_C_B $\bar{E}$ [3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV <sub>DD</sub>	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5,9,35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2,4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2
PCI1_TRDY	AG11	I/O	OV <sub>DD</sub>	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV <sub>DD</sub>	
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2
PCI1_FRAME	AE11	I/O	OV <sub>DD</sub>	2
PCI1_IDSEL	AG9	I	OV <sub>DD</sub>	
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV <sub>DD</sub>	2, 5,10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV <sub>DD</sub>	2
PCI2_CLK	AE28	I	OV <sub>DD</sub>	39
PCI2_IRDY	AD26	I/O	OV <sub>DD</sub>	2

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_PERR	AD25	I/O	OV <sub>DD</sub>	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	O	OV <sub>DD</sub>	5,9,35
PCI2_GNT0	AG25	I/O	OV <sub>DD</sub>	
PCI2_SERR	AD24	I/O	OV <sub>DD</sub>	2,4
PCI2_STOP	AF24	I/O	OV <sub>DD</sub>	2
PCI2_TRDY	AD27	I/O	OV <sub>DD</sub>	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV <sub>DD</sub>	
PCI2_REQ0	AH25	I/O	OV <sub>DD</sub>	
<b>DDR SDRAM Memory Interface</b>				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV <sub>DD</sub>	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV <sub>DD</sub>	
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV <sub>DD</sub>	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	
$\overline{\text{MDQS}}$ [0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV <sub>DD</sub>	
MBA[0:2]	F7, J7, M11	O	GV <sub>DD</sub>	
$\overline{\text{MWE}}$	E7	O	GV <sub>DD</sub>	
$\overline{\text{MCAS}}$	H7	O	GV <sub>DD</sub>	
$\overline{\text{MRAS}}$	L8	O	GV <sub>DD</sub>	
MCKE[0:3]	F10, C10, J11, H11	O	GV <sub>DD</sub>	11
$\overline{\text{MCS}}$ [0:3]	K8, J8, G8, F8	O	GV <sub>DD</sub>	
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV <sub>DD</sub>	
$\overline{\text{MCK}}$ [0:5]	J9, A15, G1, L9, B14, F2	O	GV <sub>DD</sub>	
MODT[0:3]	E6, K6, L7, M7	O	GV <sub>DD</sub>	
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36
<b>Local Bus Controller Interface</b>				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[27]	H21	O	BV <sub>DD</sub>	5,9
LA[28:31]	H20, A27, D26, A28	O	BV <sub>DD</sub>	5,7,9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV <sub>DD</sub>	
$\overline{\text{LCS5/DMA\_DREQ2}}$	D23	I/O	BV <sub>DD</sub>	1
$\overline{\text{LCS6/DMA\_DACK2}}$	G20	O	BV <sub>DD</sub>	1
$\overline{\text{LCS7/DMA\_DDONE2}}$	E21	O	BV <sub>DD</sub>	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV <sub>DD</sub>	5,9
LALE	H24	O	BV <sub>DD</sub>	5,8,9
LBCTL	G27	O	BV <sub>DD</sub>	5,8,9
LGPL0/LSDA10	F23	O	BV <sub>DD</sub>	5,9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV <sub>DD</sub>	5,9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV <sub>DD</sub>	5,8,9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV <sub>DD</sub>	5,9
LGPL4/ $\overline{\text{LGTA/LUPWAIT/LPBSE}}$	H23	I/O	BV <sub>DD</sub>	
LGPL5	E26	O	BV <sub>DD</sub>	5,9
LCKE	E24	O	BV <sub>DD</sub>	
LCLK[0:2]	E23, D24, H22	O	BV <sub>DD</sub>	
LSYNC_IN	F27	I	BV <sub>DD</sub>	
LSYNC_OUT	F28	O	BV <sub>DD</sub>	
<b>DMA</b>				
$\overline{\text{DMA\_DACK}}[0:1]$	AD3, AE1	O	OV <sub>DD</sub>	5,9,106
$\overline{\text{DMA\_DREQ}}[0:1]$	AD4, AE2	I	OV <sub>DD</sub>	
$\overline{\text{DMA\_DDONE}}[0:1]$	AD2, AD1	O	OV <sub>DD</sub>	
<b>Programmable Interrupt Controller</b>				
$\overline{\text{UDE}}$	AH16	I	OV <sub>DD</sub>	
$\overline{\text{MCP}}$	AG19	I	OV <sub>DD</sub>	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV <sub>DD</sub>	
IRQ[8]	AF19	I	OV <sub>DD</sub>	
IRQ[9]/ $\overline{\text{DMA\_DREQ3}}$	AF21	I	OV <sub>DD</sub>	1
IRQ[10]/ $\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV <sub>DD</sub>	1

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[11]/DMA_DDONE3	AD20	I/O	OV <sub>DD</sub>	1
IRQ_OUT	AD18	O	OV <sub>DD</sub>	2,4
<b>Ethernet Management Interface</b>				
EC_MDC	AB9	O	OV <sub>DD</sub>	5,9
EC_MDIO	AC8	I/O	OV <sub>DD</sub>	
<b>Gigabit Reference Clock</b>				
EC_GTX_CLK125	V11	I	LV <sub>DD</sub>	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b>				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV <sub>DD</sub>	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV <sub>DD</sub>	5, 9
TSEC1_COL	R4	I	LV <sub>DD</sub>	
TSEC1_CRS	V5	I/O	LV <sub>DD</sub>	20
TSEC1_GTX_CLK	U7	O	LV <sub>DD</sub>	
TSEC1_RX_CLK	U3	I	LV <sub>DD</sub>	
TSEC1_RX_DV	V2	I	LV <sub>DD</sub>	
TSEC1_RX_ER	T1	I	LV <sub>DD</sub>	
TSEC1_TX_CLK	T6	I	LV <sub>DD</sub>	
TSEC1_TX_EN	U9	O	LV <sub>DD</sub>	30
TSEC1_TX_ER	T7	O	LV <sub>DD</sub>	
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV <sub>DD</sub>	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV <sub>DD</sub>	
cfg_dram_type0/GPOUT6	R8	O	LV <sub>DD</sub>	5, 9
GPOUT7	N6	O	LV <sub>DD</sub>	
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV <sub>DD</sub>	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV <sub>DD</sub>	15
cfg_dram_type1	R10	I	LV <sub>DD</sub>	5

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 3)</b>				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV <sub>DD</sub>	5, 9,29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	
TSEC3_GTX_CLK	W8	O	TV <sub>DD</sub>	
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	
TSEC3_TX_EN	V9	O	TV <sub>DD</sub>	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV <sub>DD</sub>	5,9,29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV <sub>DD</sub>	
TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	31
TSEC3_TX_ER	AB6	O	TV <sub>DD</sub>	
<b>DUART</b>				
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	
UART_RTS[0:1]	AC6, AD7	O	OV <sub>DD</sub>	
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	
UART_SOUT[0:1]	AB7, AD8	O	OV <sub>DD</sub>	
<b>I<sup>2</sup>C interface</b>				
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4,27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4,27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4,27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4,27
<b>SerDes</b>				
SD_RX[0:3]	M28, N26, P28, R26	I	XV <sub>DD</sub>	
SD_RX[0:3]	M27, N25, P27, R25	I	XV <sub>DD</sub>	
SD_TX[0:3]	M22, N20, P22, R20	O	XV <sub>DD</sub>	
SD_TX[0:3]	M23, N21, P23, R21	O	XV <sub>DD</sub>	
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV <sub>DD</sub>	
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
<b>General-Purpose Output</b>				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV <sub>DD</sub>	
<b>System Control</b>				
$\overline{\text{HRESET}}$	AG17	I	OV <sub>DD</sub>	
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV <sub>DD</sub>	29
$\overline{\text{SRESET}}$	AG20	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV <sub>DD</sub>	
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV <sub>DD</sub>	2,4
<b>Debug</b>				
TRIG_IN	AB2	I	OV <sub>DD</sub>	
TRIG_OUT/READY/QUIESCE	AB1	O	OV <sub>DD</sub>	6,9,19,29
MSRCID[0:1]	AE4, AG2	O	OV <sub>DD</sub>	5,6,9
MSRCID[2:4]	AF3, AF1, AF2	O	OV <sub>DD</sub>	6,19,29
MDVAL	AE5	O	OV <sub>DD</sub>	6
CLK_OUT	AE21	O	OV <sub>DD</sub>	11
<b>Clock</b>				
RTC	AF16	I	OV <sub>DD</sub>	
SYSCLK	AH17	I	OV <sub>DD</sub>	
<b>JTAG</b>				
TCK	AG28	I	OV <sub>DD</sub>	
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	O	OV <sub>DD</sub>	11
TMS	AH27	I	OV <sub>DD</sub>	12
$\overline{\text{TRST}}$	AH23	I	OV <sub>DD</sub>	12

**Table 69. MPC8545E Pinout Listing (continued)**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>DFT</b>				
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV <sub>DD</sub>	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV <sub>DD</sub>	25
<b>Thermal Management</b>				
THERM0	AG1		—	14
THERM1	AH1		—	14
<b>Power Management</b>				
ASLEEP	AH18	O	OV <sub>DD</sub>	9,19,29
<b>Power and Ground Signals</b>				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27 K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28 L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21 U27	—	—	
OVDD	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3V)	OVDD	
LVDD	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5V, 3.3V)	LVDD	
TVDD	W9, Y6	Power for TSEC3 and TSEC4 (2.5V, 3.3V)	TVDD	



Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V, 2.5V)	GVDD	
BVDD	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	
VDD	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for Core (1.1 V)	VDD	
SVDD	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SVDD	
XVDD	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XVDD	
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)		26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)		26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)		26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	O	V <sub>DD</sub>	13
SENSEVSS	M16			13

Table 69. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Analog Signals</b>				
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	O		24

**Notes:**

All note references in this table use the same numbers as those for [Table 67](#). The reader should refer to [Table 67](#) for the meanings of these notes.

[Table 70](#) provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

**NOTE**

All note references in the following table use the same numbers as those for [Table 67](#). The reader should refer to [Table 67](#) for the meanings of these notes.

Table 70. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 (one 32-bit)</b>				
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	—	—	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	O	OV <sub>DD</sub>	
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV <sub>DD</sub>	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
Reserved	AF15, AD14, AE15, AD15	—	—	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
Reserved	W15	—	—	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5,9,35

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PCI1\_GNT0}}$	AG5	I/O	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_IRDY}}$	AF11	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_PAR}}$	AD12	I/O	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	$\text{OV}_{\text{DD}}$	2,4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_TRDY}}$	AG11	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_REQ}}[4:1]$	AH2, AG4, AG3, AH4	I	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_REQ0}}$	AH3	I/O	$\text{OV}_{\text{DD}}$	
$\overline{\text{PCI1\_CLK}}$	AH26	I	$\text{OV}_{\text{DD}}$	39
$\overline{\text{PCI1\_DEVSEL}}$	AH11	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_FRAME}}$	AE11	I/O	$\text{OV}_{\text{DD}}$	2
$\overline{\text{PCI1\_IDSEL}}$	AG9	I	$\text{OV}_{\text{DD}}$	
cfg_pci1_width	AF14	I/O	$\text{OV}_{\text{DD}}$	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	$\text{OV}_{\text{DD}}$	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
<b>DDR SDRAM Memory Interface</b>				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	$\text{GV}_{\text{DD}}$	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	$\text{GV}_{\text{DD}}$	

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV <sub>DD</sub>	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	
$\overline{\text{MDQS}}$ [0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV <sub>DD</sub>	
MBA[0:2]	F7, J7, M11	O	GV <sub>DD</sub>	
$\overline{\text{MWE}}$	E7	O	GV <sub>DD</sub>	
$\overline{\text{MCAS}}$	H7	O	GV <sub>DD</sub>	
$\overline{\text{MRAS}}$	L8	O	GV <sub>DD</sub>	
MCKE[0:3]	F10, C10, J11, H11	O	GV <sub>DD</sub>	11
$\overline{\text{MCS}}$ [0:3]	K8, J8, G8, F8	O	GV <sub>DD</sub>	
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV <sub>DD</sub>	
$\overline{\text{MCK}}$ [0:5]	J9, A15, G1, L9, B14, F2	O	GV <sub>DD</sub>	
MODT[0:3]	E6, K6, L7, M7	O	GV <sub>DD</sub>	
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36
<b>Local Bus Controller Interface</b>				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	
LA[27]	H21	O	BV <sub>DD</sub>	5,9
LA[28:31]	H20, A27, D26, A28	O	BV <sub>DD</sub>	5,7,9
$\overline{\text{LCS}}$ [0:4]	J25, C20, J24, G26, A26	O	BV <sub>DD</sub>	
$\overline{\text{LCS5/DMA\_DREQ2}}$	D23	I/O	BV <sub>DD</sub>	1
$\overline{\text{LCS6/DMA\_DACK2}}$	G20	O	BV <sub>DD</sub>	1
$\overline{\text{LCS7/DMA\_DDONE2}}$	E21	O	BV <sub>DD</sub>	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV <sub>DD</sub>	5,9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV <sub>DD</sub>	5,9
LALE	H24	O	BV <sub>DD</sub>	5,8,9
LBCTL	G27	O	BV <sub>DD</sub>	5,8,9
LGPL0/LSDA10	F23	O	BV <sub>DD</sub>	5,9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV <sub>DD</sub>	5,9

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL2/LOE/LSDRAS	B27	O	BV <sub>DD</sub>	5,8,9
LGPL3/LSDCAS	F24	O	BV <sub>DD</sub>	5,9
LGPL4/LGTĀ/LUPWAIT/LPBSE	H23	I/O	BV <sub>DD</sub>	
LGPL5	E26	O	BV <sub>DD</sub>	5,9
LCKE	E24	O	BV <sub>DD</sub>	
LCLK[0:2]	E23, D24, H22	O	BV <sub>DD</sub>	
LSYNC_IN	F27	I	BV <sub>DD</sub>	
LSYNC_OUT	F28	O	BV <sub>DD</sub>	
<b>DMA</b>				
DMA_DACK[0:1]	AD3, AE1	O	OV <sub>DD</sub>	5,9,108
DMA_DREQ[0:1]	AD4, AE2	I	OV <sub>DD</sub>	
DMA_DDONE[0:1]	AD2, AD1	O	OV <sub>DD</sub>	
<b>Programmable Interrupt Controller</b>				
UDE	AH16	I	OV <sub>DD</sub>	
MCP	AG19	I	OV <sub>DD</sub>	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV <sub>DD</sub>	
IRQ[8]	AF19	I	OV <sub>DD</sub>	
IRQ[9]/DMA_DREQ3	AF21	I	OV <sub>DD</sub>	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV <sub>DD</sub>	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV <sub>DD</sub>	1
IRQ_OUT	AD18	O	OV <sub>DD</sub>	2,4
<b>Ethernet Management Interface</b>				
EC_MDC	AB9	O	OV <sub>DD</sub>	5,9
EC_MDIO	AC8	I/O	OV <sub>DD</sub>	
<b>Gigabit Reference Clock</b>				
EC_GTX_CLK125	V11	I	LV <sub>DD</sub>	
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b>				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV <sub>DD</sub>	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV <sub>DD</sub>	5, 9
TSEC1_COL	R4	I	LV <sub>DD</sub>	
TSEC1_CRS	V5	I/O	LV <sub>DD</sub>	20
TSEC1_GTX_CLK	U7	O	LV <sub>DD</sub>	

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_CLK	U3	I	LV <sub>DD</sub>	
TSEC1_RX_DV	V2	I	LV <sub>DD</sub>	
TSEC1_RX_ER	T1	I	LV <sub>DD</sub>	
TSEC1_TX_CLK	T6	I	LV <sub>DD</sub>	
TSEC1_TX_EN	U9	O	LV <sub>DD</sub>	30
TSEC1_TX_ER	T7	O	LV <sub>DD</sub>	
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV <sub>DD</sub>	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV <sub>DD</sub>	
cfg_dram_type0/GPOUT6	R8	O	LV <sub>DD</sub>	5, 9
GPOUT7	N6	O	LV <sub>DD</sub>	
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV <sub>DD</sub>	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV <sub>DD</sub>	15
cfg_dram_type1	R10	O	LV <sub>DD</sub>	5, 9
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 3)</b>				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV <sub>DD</sub>	5, 9,29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	
TSEC3_GTX_CLK	W8	O	TV <sub>DD</sub>	
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	
TSEC3_TX_EN	V9	O	TV <sub>DD</sub>	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV <sub>DD</sub>	5,9,29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV <sub>DD</sub>	
TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	31
TSEC3_TX_ER	AB6	O	TV <sub>DD</sub>	

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>DUART</b>				
$\overline{\text{UART\_CTS}}[0:1]$	AB3, AC5	I	$\text{OV}_{\text{DD}}$	
$\overline{\text{UART\_RTS}}[0:1]$	AC6, AD7	O	$\text{OV}_{\text{DD}}$	
UART_SIN[0:1]	AB5, AC7	I	$\text{OV}_{\text{DD}}$	
UART_SOUT[0:1]	AB7, AD8	O	$\text{OV}_{\text{DD}}$	
<b>I<sup>2</sup>C interface</b>				
IIC1_SCL	AG22	I/O	$\text{OV}_{\text{DD}}$	4,27
IIC1_SDA	AG21	I/O	$\text{OV}_{\text{DD}}$	4,27
IIC2_SCL	AG15	I/O	$\text{OV}_{\text{DD}}$	4,27
IIC2_SDA	AG14	I/O	$\text{OV}_{\text{DD}}$	4,27
<b>SerDes</b>				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	$\text{XV}_{\text{DD}}$	
$\overline{\text{SD\_RX}}[0:7]$	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	$\text{XV}_{\text{DD}}$	
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	$\text{XV}_{\text{DD}}$	
$\overline{\text{SD\_TX}}[0:7]$	M23, N21, P23, R21, U21, V23, W21, Y23	O	$\text{XV}_{\text{DD}}$	
SD_PLL_TPD	U28	O	$\text{XV}_{\text{DD}}$	24
SD_REF_CLK	T28	I	$\text{XV}_{\text{DD}}$	
$\overline{\text{SD\_REF\_CLK}}$	T27	I	$\text{XV}_{\text{DD}}$	
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
<b>General-Purpose Output</b>				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	$\text{BV}_{\text{DD}}$	
<b>System Control</b>				
HRESET	AG17	I	$\text{OV}_{\text{DD}}$	
HRESET_REQ	AG16	O	$\text{OV}_{\text{DD}}$	29
SRESET	AG20	I	$\text{OV}_{\text{DD}}$	
CKSTP_IN	AA9	I	$\text{OV}_{\text{DD}}$	
$\overline{\text{CKSTP\_OUT}}$	AA8	O	$\text{OV}_{\text{DD}}$	2,4
<b>Debug</b>				
TRIG_IN	AB2	I	$\text{OV}_{\text{DD}}$	
TRIG_OUT/READY/QUIESCE	AB1	O	$\text{OV}_{\text{DD}}$	6,9,19,29

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MSRCID[0:1]	AE4, AG2	O	OV <sub>DD</sub>	5,6,9
MSRCID[2:4]	AF3, AF1, AF2	O	OV <sub>DD</sub>	6,19,29
MDVAL	AE5	O	OV <sub>DD</sub>	6
CLK_OUT	AE21	O	OV <sub>DD</sub>	11
<b>Clock</b>				
RTC	AF16	I	OV <sub>DD</sub>	
SYSCLK	AH17	I	OV <sub>DD</sub>	
<b>JTAG</b>				
TCK	AG28	I	OV <sub>DD</sub>	
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	O	OV <sub>DD</sub>	11
TMS	AH27	I	OV <sub>DD</sub>	12
$\overline{\text{TRST}}$	AH23	I	OV <sub>DD</sub>	12
<b>DFT</b>				
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV <sub>DD</sub>	25
TEST_SEL	AH14	I	OV <sub>DD</sub>	109
<b>Thermal Management</b>				
THERM0	AG1		—	14
THERM1	AH1		—	14
<b>Power Management</b>				
ASLEEP	AH18	O	OV <sub>DD</sub>	9,19,29



Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Power and Ground Signals</b>				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27 K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28 L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21 U27	—	—	
OVDD	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3V)	OVDD	
LVDD	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5V, 3.3V)	LVDD	
TVDD	W9, Y6	Power for TSEC3 and TSEC4 (2.5V, 3.3V)	TVDD	
GVDD	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V, 2.5V)	GVDD	
BVDD	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	
VDD	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for Core (1.1 V)	VDD	
SVDD	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SVDD	

Table 70. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XVDD	
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)		26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)		26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)		26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	O	V <sub>DD</sub>	13
SENSEVSS	M16			13
<b>Analog Signals</b>				
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	O		24

**Notes:**

All note references in this table use the same numbers as those for [Table 67](#). The reader should refer to [Table 67](#) for the meanings of these notes.

# 19 Clocking

This section describes the PLL configuration of the MPC8548E. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 19.1 Clock Ranges

Table 71, Table 72, and Table 73 provide the clocking specifications for the processor cores and Table 74, Table 75, and Table 76 provide the clocking specifications for the memory bus.

**Table 71. Processor Core Clocking Specifications (MPC8548E and MPC8547E)**

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1000 MHz		1200 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	533	1000	533	1200	533	1333	MHz	1, 2

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, "CCB/SYSCLK PLL Ratio,"](#) and [Section 19.3, "e500 Core PLL Ratio,"](#) for ratio settings.
- The minimum e500 core frequency is based on the minimum platform frequency of 266 MHz.

**Table 72. Processor Core Clocking Specifications (MPC8545E)**

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	533	800	533	1000	533	1200	MHz	1, 2

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, "CCB/SYSCLK PLL Ratio,"](#) and [Section 19.3, "e500 Core PLL Ratio,"](#) for ratio settings.
- The minimum e500 core frequency is based on the minimum platform frequency of 266 MHz.

**Table 73. Processor Core Clocking Specifications (MPC8543E)**

Characteristic	Maximum Processor Core Frequency				Unit	Notes
	800 MHz		1000 MHz			
	Min	Max	Min	Max		
e500 core processor frequency	533	800	533	1000	MHz	1, 2

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- The minimum e500 core frequency is based on the minimum platform frequency of 266 MHz.

**Table 74. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)**

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1200, 1333 MHz			
	Min	Max		
Memory bus clock speed	133	266	MHz	1, 2

**Notes:**

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

**Table 75. Memory Bus Clocking Specifications (MPC8545E)**

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1200 MHz			
	Min	Max		
Memory bus clock speed	133	200	MHz	1, 2

**Notes:**

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

**Table 76. Memory Bus Clocking Specifications (MPC8543E)**

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000 MHz			
	Min	Max		
Memory bus clock speed	133	200	MHz	1, 2

**Notes:**

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

## 19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in [Table 77](#):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI\_CLK, refer to the PCI 2.2 Specification.

**Table 77. CCB Clock Ratio**

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	20:1
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

## 19.3 e500 Core PLL Ratio

[Table 78](#) describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in [Table 78](#).

**Table 78. e500 Core to CCB Clock Ratio**

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

## 19.4 Frequency Options

### 19.4.1 Sysclk to Platform Frequency Options

Table 79 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

**Table 79. Frequency Options of SYSCLK with Respect to Memory Bus Speeds**

CCB to SYSCLK Ratio	SYSCLK (MHz)									
	16.66	25	33.33	41.66	66.66	83	100	111	133.33	166
	Platform /CCB Frequency (MHz)									
2										333
3								333	400	498
4						333	400	445	533	
5					333	415	500			
6					400	500				
8				333	533					
9				375						
10			333	417						
12		300	400	500						
16		400	533							
20	333	500								

## 20 Thermal

This section describes the thermal specifications of the MPC8548.

### 20.1 Thermal for Version 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

Table 80 shows the package thermal characteristics.

**Table 80. Package Thermal Characteristics for HiCTE FC-CBGA**

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die Junction-to-Ambient (Natural Convection)	Single-layer board (1s)	$R_{\theta JA}$	17	°C/W	1,2
Die Junction-to-Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1,2
Die Junction-to-Ambient (200 ft/min)	Single-layer board (1s)	$R_{\theta JA}$	11	°C/W	1,2
Die Junction-to-Ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\theta JA}$	8	°C/W	1,2
Die Junction-to-Board	N/A	$R_{\theta JB}$	3	°C/W	3
Die Junction-to-Case	N/A	$R_{\theta JC}$	0.8	°C/W	4

**NOTES:**

- 1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2 Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

### 20.2 Thermal for Version 2.1 Silicon FC-PBGA with Full Lid

This section describes the thermal specifications for the FC-PBGA package for revision 2.1 silicon.

Table 81 shows the package thermal characteristics.

**Table 81. Package Thermal Characteristics for FC-PBGA**

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die Junction-to-Ambient (Natural Convection)	Single-layer board (1s)	$R_{\theta JA}$	18	°C/W	1,2
Die Junction-to-Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\theta JA}$	13	°C/W	1,2
Die Junction-to-Ambient (200 ft/min)	Single-layer board (1s)	$R_{\theta JA}$	13	°C/W	1,2

**Table 81. Package Thermal Characteristics for FC-PBGA**

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die Junction-to-Ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1,2
Die Junction-to-Board	N/A	$R_{\theta JB}$	5	°C/W	3
Die Junction-to-Case	N/A	$R_{\theta JC}$	0.8	°C/W	4

**NOTES:**

- 1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2 Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

## 20.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed circuit board is the recommended procedure using a maximum of 10 lbs. force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

## 21 System Design Information

This section provides electrical design recommendations for successful application of the MPC8548E.

### 21.1 System Clocking

This device includes five PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 19.2, “CCB/SYSCLK PLL Ratio.”](#)
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 19.3, “e500 Core PLL Ratio.”](#)
3. The PCI PLL generates the clocking for the PCI bus
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.



## 21.2 Power Supply Design

### 21.2.1 PLL Power Supply Filtering

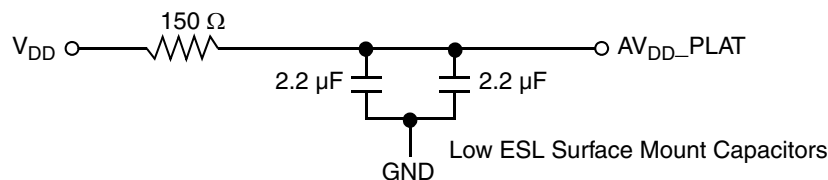
Each of the PLLs listed above is provided with power through independent power supply pins ( $AV_{DD\_PLAT}$ ,  $AV_{DD\_CORE}$ ,  $AV_{DD\_PCI}$ ,  $AV_{DD\_LBIU}$ , and  $AV_{DD\_SRDS}$  respectively). The  $AV_{DD}$  level should always be equivalent to  $V_{DD}$ , and preferably these voltages will be derived directly from  $V_{DD}$  through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 47](#), one to each of the  $AV_{DD}$  pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

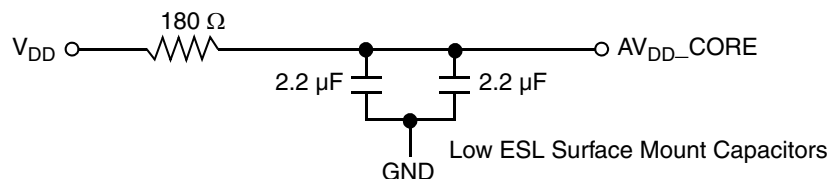
This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific  $AV_{DD}$  pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of the footprint, without the inductance of vias.

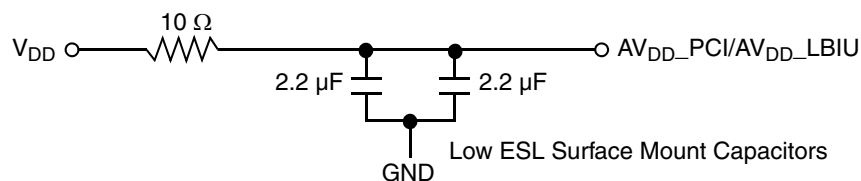
[Figure 47](#) through [Figure 49](#) shows the PLL power supply filter circuits.



**Figure 47. PLL Power Supply Filter Circuit with PLAT Pins**

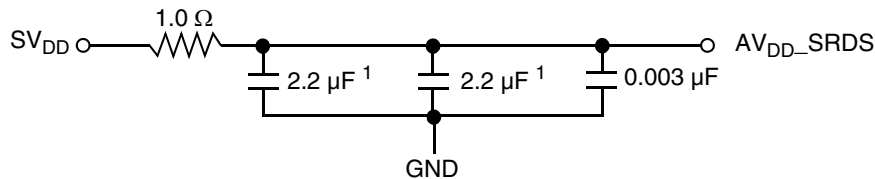


**Figure 48. PLL Power Supply Filter Circuit with CORE Pins**



**Figure 49. PLL Power Supply Filter Circuit with PCI/LBIU Pins**

The  $AV_{DD\_SRDS}$  signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the  $AV_{DD\_SRDS}$  ball to ensure it filters out as much noise as possible. The ground connection should be near the  $AV_{DD\_SRDS}$  ball. The  $0.003\text{-}\mu\text{F}$  capacitor is closest to the ball, followed by the two  $2.2\text{ }\mu\text{F}$  capacitors, and finally the  $1\text{ }\Omega$  resistor to the board supply plane. The capacitors are connected from  $AV_{DD\_SRDS}$  to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 50. SerDes PLL Power Supply Filter**

Note the following:

- $AV_{DD\_SRDS}$  should be a filtered version of  $SV_{DD}$ .
- Signals on the SerDes interface are fed from the  $XV_{DD}$  power plane.
- Power:  $XV_{DD}$  consumes less than 300 mW;  $SV_{DD} + AV_{DD\_SRDS}$  consumes less than 750 mW.

## 21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8548E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each  $V_{DD}$ ,  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$ , pin of the device. These decoupling capacitors should receive their power from separate  $V_{DD}$ ,  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$ , and  $GND$  power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of  $0.01$  or  $0.1\ \mu\text{F}$ . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the  $V_{DD}$ ,  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$ , planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors— $100\text{--}330\ \mu\text{F}$  (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

## 21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ( $SV_{DD}$  and  $XV_{DD}$ ) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- $\mu$ F ceramic chip capacitor from each SerDes supply ( $SV_{DD}$  and  $XV_{DD}$ ) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10- $\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- $\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to  $V_{DD}$ ,  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$ , as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external  $V_{DD}$ ,  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$ , and GND pins of the device.

## 21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8548E requires weak pull-up resistors (2–10 k $\Omega$  is recommended) on open drain type pins including I<sup>2</sup>C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 53](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3\_TXD[3], HRESET\_REQ, TRIG\_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA\_DACK[0:1] and TEST\_SEL/TEST\_SEL pins must be set to a proper state during POR configuration. Please refer to the pinlist table of the individual device for more details

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

## 21.7 Output Buffer DC Impedance

The MPC8548E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I<sup>2</sup>C).

To measure  $Z_0$  for the single-ended drivers, an external resistor is connected from the chip pad to  $OV_{DD}$  or GND. Then, the value of each resistor is varied until the pad voltage is  $OV_{DD}/2$  (see Figure 51). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N)/2$ .

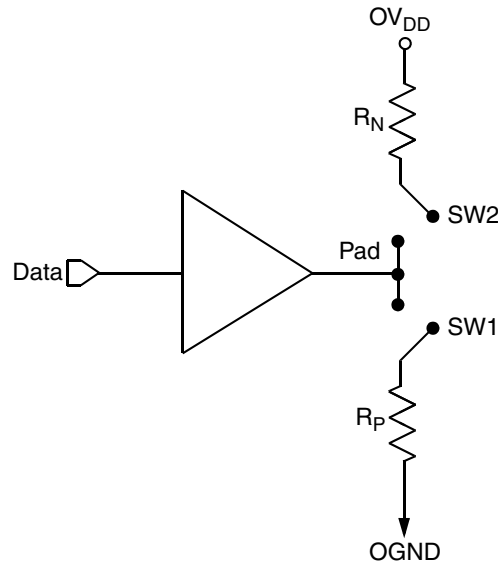


Figure 51. Driver Impedance Measurement

Table 82 summarizes the signal impedance targets. The driver impedances are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

Table 82. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
$R_N$	43 Target	25 Target	20 Target	$Z_0$	W
$R_P$	43 Target	25 Target	20 Target	$Z_0$	W

Note: Nominal supply voltages. See Table 1,  $T_j = 105^\circ\text{C}$ .

## 21.8 Configuration Pin Muxing

The MPC8548E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k $\Omega$ . This value should permit the 4.7-k $\Omega$  resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform /system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 53](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The  $\overline{\text{TRST}}$  signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires  $\overline{\text{TRST}}$  to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert  $\overline{\text{TRST}}$  during the power-on reset flow. Simply tying  $\overline{\text{TRST}}$  to  $\overline{\text{HRESET}}$  is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$  in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 53](#) allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in [Figure 52](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

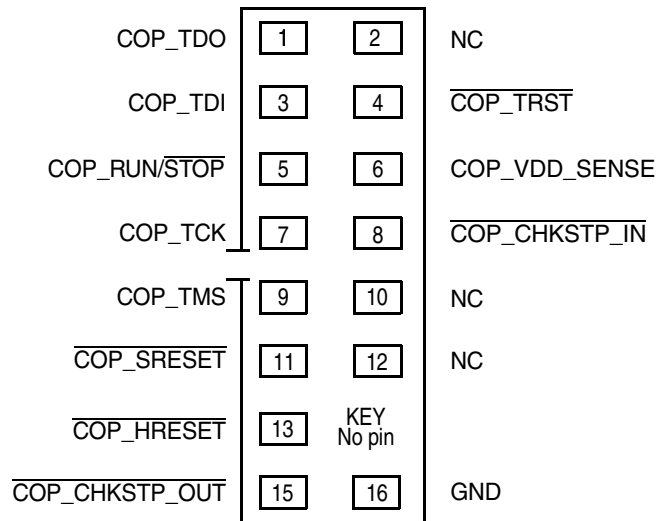
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 52](#) is common to all known emulators.

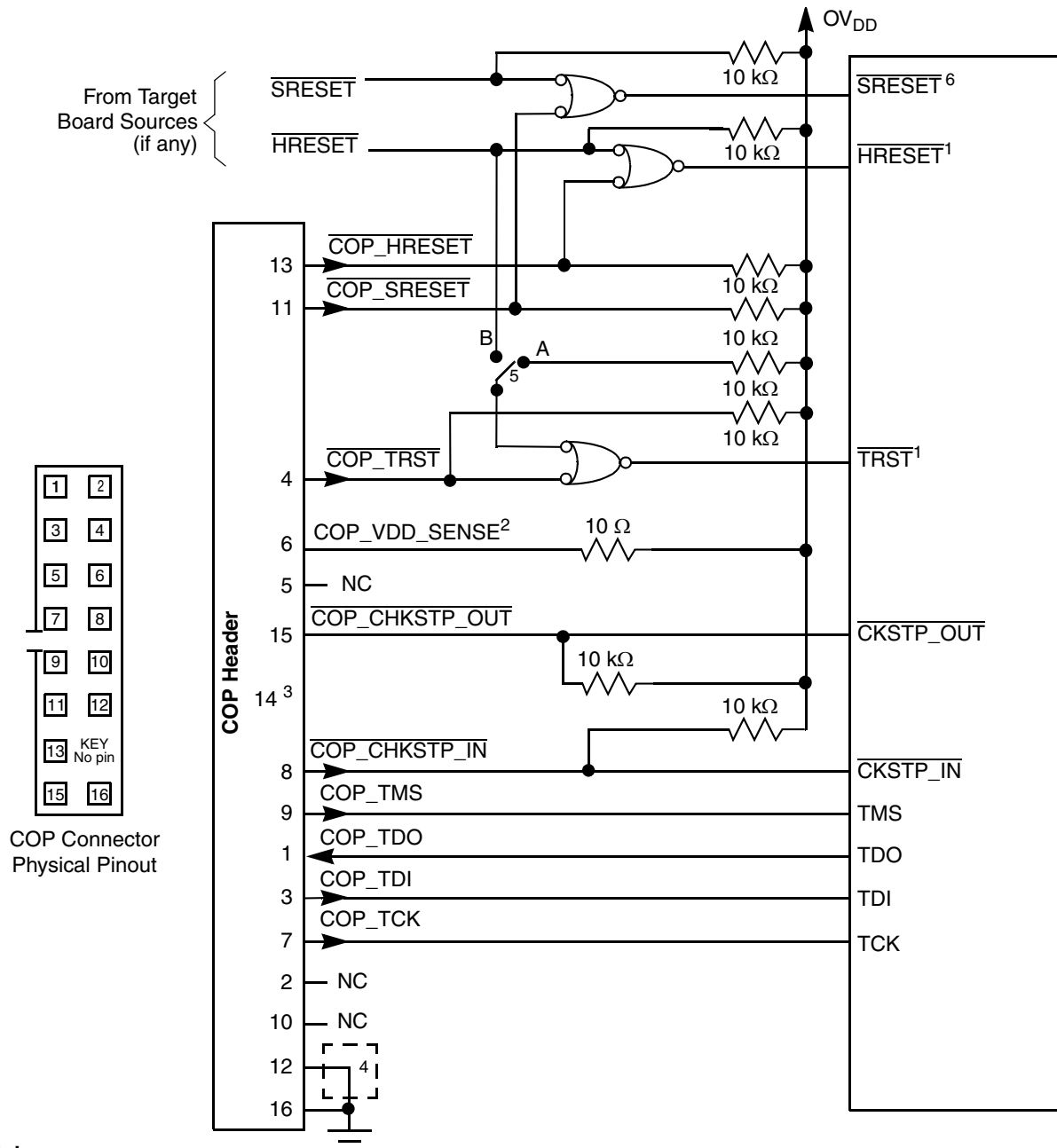
## 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$  should be tied to  $\overline{\text{HRESET}}$  through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal ( $\overline{\text{HRESET}}$ ) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor will allow future access to  $\overline{\text{TRST}}$  in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



**Figure 52. COP Connector Physical Pinout**



**Notes:**

1. The COP port and target board should be able to independently assert  $\overline{\text{HRESET}}$  and  $\overline{\text{TRST}}$  to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the  $\overline{\text{TRST}}$  line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting  $\overline{\text{SRESET}}$  causes a machine check interrupt to the e500 core.

**Figure 53. JTAG Interface Connection**



## 21.10 Guidelines for High-Speed Interface Termination

### 21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD\_TX[7:0]
- $\overline{\text{SD\_TX}}[7:0]$
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD\_RX[7:0]
- $\overline{\text{SD\_RX}}[7:0]$
- SD\_REF\_CLK
- $\overline{\text{SD\_REF\_CLK}}$

#### NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE\_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to  $XV_{DD}$ . Pins V27 and M25 must be tied to GND through a 300- $\Omega$  resistor.

In Rev 2.0 silicon, POR configuration pin `cfg_srds_en` on TSEC4\_TXD[2] /TSEC3\_TXD[6] can be used to power down SerDes block.

### 21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD\_TX[7:0]
- $\overline{\text{SD\_TX}}[7:0]$
- reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD\_RX[7:0]
- $\overline{\text{SD\_RX}}[7:0]$
- SD\_REF\_CLK
- $\overline{\text{SD\_REF\_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE\_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XVDD. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

## 21.11 Guideline for PCI Interface Termination

PCI termination if PCI 1 or PCI 2 is not used at all.

### Option 1

If PCI arbiter is enabled during POR,

- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to  $OV_{DD}$  through a single 10K ohm resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

### Option 2

If PCI arbiter is disabled during POR,

- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to  $OV_{DD}$  through a single (or multiple) 10K ohm resistor(s)
- All PCI control pins can be grouped together and tied to  $OV_{DD}$  through a single 10K resistor
- It is optional to disable PCI block through DEVDISR register after POR reset.

## 21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used. Here is the termination recommendation:

For LDP[0:3]: tie them to ground or the power supply rail via a 4.7K resistor.

For LPBSE: tie it to the power supply rail via a 4.7K resistor (pull-up resistor).

## 22 Document Revision History

Table 98 provides a revision history for the MPC8548E hardware specification.

**Table 83. Document Revision History**

Revision	Date	Substantive Change(s)
2	4/2008	<ul style="list-style-type: none"> <li>Removed 1:1 support on Table 78, “e500 Core to CCB Clock Ratio.</li> <li>Removed MDM from Table 18, “DDR SDRAM Input AC Timing Specifications. MDM is an Output.</li> <li>Figure 47, “PLL Power Supply Filter Circuit with PLAT Pins” (AVDD_PLAT)</li> <li>Figure 48, “PLL Power Supply Filter Circuit with CORE Pins” (AVDD_CORE)</li> <li>Split Figure 49, “PLL Power Supply Filter Circuit with PCI/LBIU Pins,” (formerly called just “PLL Power Supply Filter Circuit”) into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones:</li> </ul>
1	10/2007	<ul style="list-style-type: none"> <li>Adjusted maximum SYSCLK frequency down in Table 6, “SYSCLK AC Timing Specifications” per device erratum GEN-13</li> <li>Clarified notes to Table 7, “EC_GTX_CLK125 AC Timing Specifications”</li> <li>Added Section 4.4, “PCI/PCI-X Reference Clock Timing”</li> <li>Clarified descriptions and added PCI/PCI-X to Table 10, “PLL Lock Times”</li> <li>Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, “DDR and DDR2 SDRAM”</li> <li>Clarified Note 4 of Table 19, “DDR SDRAM Output AC Timing Specifications”</li> <li>Clarified the reference clock used in Section 7.2, “DUART AC Electrical Specifications”</li> <li>Corrected <math>V_{IH}(\text{min})</math> in Table 22, “GMII, MII, RMII, and TBI DC Electrical Characteristics”</li> <li>Corrected <math>V_{IL}(\text{max})</math> in Table 23, “RGMII, RTBI, and FIFO DC Electrical Characteristics”</li> <li>Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35</li> <li>Corrected <math>V_{IH}(\text{min})</math> in Table 36, “MII Management DC Electrical Characteristics”</li> <li>Corrected <math>t_{MDC}(\text{min})</math> in Table 37, “MII Management AC Timing Specifications”</li> <li>Updated parameter descriptions for <math>t_{LBIVKH1}</math>, <math>t_{LBIVKH2}</math>, <math>t_{LBIXKH1}</math>, and <math>t_{LBIXKH2}</math> in Table 40, “Local Bus Timing Parameters (<math>BV_{DD} = 3.3 \text{ V}</math>)—PLL Enabled” and Table 41, “Local Bus Timing Parameters (<math>BV_{DD} = 2.5 \text{ V}</math>)—PLL Enabled”</li> <li>Updated parameter descriptions for <math>t_{LBIVKH1}</math>, <math>t_{LBIVKL2}</math>, <math>t_{LBIXKH1}</math>, and <math>t_{LBIXKL2}</math> in Table 42, “Local Bus Timing Parameters—PLL Bypassed.” Note that <math>t_{LBIVKL2}</math> and <math>t_{LBIXKL2}</math> were previously labeled <math>t_{LBIVKH2}</math> and <math>t_{LBIXKH2}</math></li> <li>Added LUPWAIT signal to Figure 23, “Local Bus Signals (PLL Enabled)” and Figure 24, “Local Bus Signals (PLL Bypass Mode)”</li> <li>Added <math>\overline{LGTA}</math> signal to Figure 25, Figure 26, Figure 27 and Figure 28</li> <li>Corrected LUPWAIT assertion in Figure 26 and Figure 28</li> <li>Clarified the PCI reference clock in Section 14.2, “PCI/PCI-X AC Electrical Specifications”</li> <li>Updated Figure 38, “Driver and Receiver of SerDes (PCI Express, Serial RapidIO, and SD_REF_CLK/SD_REF_CLK)”</li> <li>Added Section 18.1, “Package Parameters”</li> <li>Added PBGA thermal information in Section 20.2, “Thermal for Version 2.1 Silicon FC-PBGA with Full Lid”</li> <li>Updated Section 20.3, “Heat Sink Solution”</li> <li>Updated Table 84, “Part Numbering Nomenclature”</li> </ul>
0	7/2007	<ul style="list-style-type: none"> <li>Initial Release</li> </ul>

## 23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 23.1, “Part Numbers Fully Addressed by this Document.”](#)

### 23.1 Part Numbers Fully Addressed by this Document

[Table 84](#) provides the Freescale part numbering nomenclature for the MPC8548E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 84. Part Numbering Nomenclature

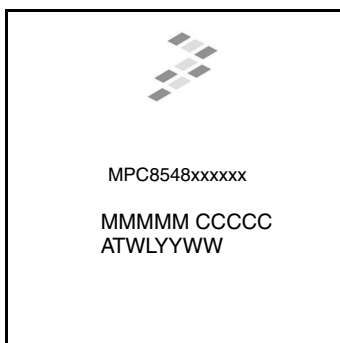
MPC	nnnnn	t	pp	ff	c	r	
Product Code	Part Identifier	Temperature	Package <sup>1,2,3</sup>	Processor Frequency <sup>4</sup>	Core Frequency	Silicon Version	
MPC	8548E	Blank = 0 to 105°C C = -40 to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 <sup>3</sup> AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 <sup>5</sup> G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1 (SVR = 0x80390021)	
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1 (SVR = 0x80310021)	
	8547E					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1 (SVR = 0x80390121)	
	8545E				AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1 (SVR = 0x80390221)
	8545						Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1 (SVR = 0x80310221)
	8543E				AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1 (SVR = 0x803A0021)
	8543						Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1 (SVR = 0x80320021)

**Notes:**

1. See [Section 18, "Package Description,"](#) for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.

## 23.2 Part Marking

Parts are marked as the example shown in [Figure 54](#).



**Notes:**

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 54. Part Marking for CBGA and PBGA Device**



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